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# Developments in 300mm Low-Power Si Capacitive Modulators

*Invited paper*

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## ABSTRACT

We report on the development of high speed phase shifters for next generation of Si photonics transceivers, based on capacitive structures. Experimental measurements show a  $V_{\pi}L_{\pi}$  of 0.5V.cm in accumulation regime. We also show that the addition of a SiGe layer at the capacitive interface leads to an improvement of 25 % of the phase shifter efficiency.

**Keywords:** Silicon capacitive modulators, damascene process, poly silicon, SiGe booster

## INTRODUCTION

Silicon photonics has emerged industrially more than a decade ago and is now a well-established technology. Currently, the main application addressed is data-communication, essentially providing active optical transceiver cables for data-centres and metro interconnection networks. The vast deployment of data-centres across the World and its expansion into hyper-data-centres triggers the needs to increase the data-rate transmission, improve the power consumption efficiency and reduce optical signal losses to achieve faster and longer-reach cables.

A key component used in silicon photonics is the modulator found in the transmitter section. It consists of applying a signal amplitude modulation on the optical carrier using an electro-optical effect. PN junctions put in a Mach-Zehnder interferometer (MZI) configuration are the common components used to perform that operation. However, the poor electro-optical efficiency of the diodes result in millimetre long MZI sub-systems. High power consumption of the electronic driver, which controls the MZI diodes, is the principal consequence of that low-efficiency and high footprint [1].

In this paper, we propose a new electro-optical device architecture based on a capacitive structure. Various experimental studies were reported on capacitive structures in silicon platforms [3], [4], [4]. However, our focus is to integrate the device within a transceiver system. We develop a fabrication scheme that makes it possible to co-integrate a Crystal-Si, Oxide, Poly-Si Accumulator (COPA) with other active devices such as Si pn and pin junctions, Ge photodiodes and a complex, 4 layer electrical interconnection back-end of line (BEOL). Our strategy is to insert a new process module within in photonics fabrication flow without any alteration to other devices.

## 1. CAPACITIVE MODULATOR DESIGN

Figure 1a-b shows the capacitive phase-shifter cross-section. The COPA structure is formed by a P-doped crystalline Si layer, on top of which SiO<sub>2</sub> and N-doped poly Si layers are deposited. As a function of the voltage applied on the P<sup>+</sup>/N<sup>+</sup> contacts, carrier accumulation occurs around the oxide layer, leading to refractive index variations in the centre of the waveguide, and phase modulation of the guided mode. The performances of the COPA structure are simulated by solving Poisson equation within Synopsys Device module [5] and the optical mode profile with Lumerical MODE [6]. The impact of the oxide thickness (noted  $t_{ox}$ ) and the doping levels (D) are simulated. The  $t_{ox}$  variation is between [5 – 15]nm and D between [5.2E<sup>17</sup> - 1.7E<sup>18</sup>]cm<sup>-3</sup>. The voltage swing  $V_{pp}$  is of only 0.9V to ensure low power consumption. Previous simulations indicated that the best efficiency is thus obtained for an applied voltage between [0.9 – 1.8]V, keeping the capacitive structure in the accumulation regime.

To evaluate the phase shifter performance, the optical modulation amplitude (OMA) is considered. It depends on the phase shift per unit length  $\Delta\phi$  (rad/mm), and on the optical loss per unit length  $\alpha$  (mm<sup>-1</sup>). For an optical input power of 1mW, the OMA of a L-long phase shifter is given by (1).

$$\text{OMA} = e^{-\alpha L} |\sin(L \cdot \Delta\phi)| \quad (1)$$

From (1) we can see that OMA depends on the phase shifter length. From the derivative of (1), we can deduce the optimal length  $L_{\text{opt}}$  that maximizes OMA [7]:

$$L_{\text{opt}} = \frac{1}{\Delta\phi} \cdot \text{atan}\left(\frac{\Delta\phi}{\alpha}\right) \quad (2)$$

Figure 1c shows the evolution of  $\Delta\phi$  and  $L_{\text{opt}}$  as a function of  $D$  and  $t_{\text{ox}}$ . The largest phase shift efficiency are obtained for thin oxide and for the lowest values of the doping level. However higher  $D$  reduces the device footprint, while device speed which is limited by RC product decreases when the oxide thickness and doping level decreases. The operating range for 25 Gbit/s and 56 Gbit/s are coloured in Fig 1c, showing that  $t_{\text{ox}} \geq 7\text{nm}$  and  $t_{\text{ox}} \geq 12\text{nm}$  are required for 25 Gbit/s and 56 Gbit/s respectively.

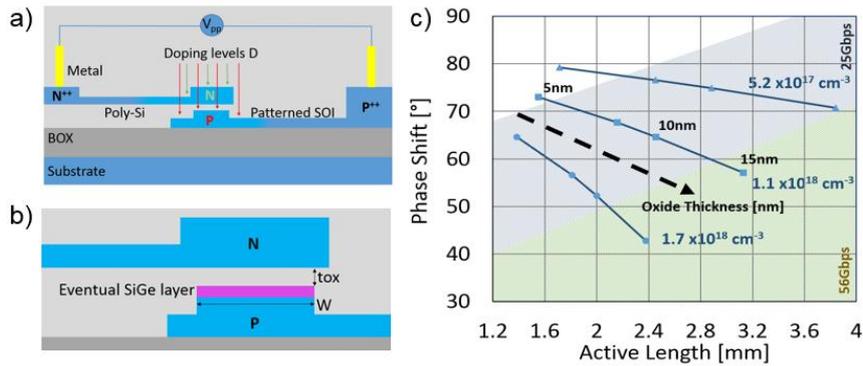


Figure 1: (a) Phase-shifter cross-section showing the capacitive structure. (b) Detailed cross-section of the COPA waveguide. A thin layer of p-type SiGe can eventually be grown above the SOI layer. (c) Simulated features of the capacitive structure.

## 2. FABRICATION PROCESS

The fabrication scheme has been defined in order to be able to co-integrate the COPA structure with the other active devices already present in Si transceivers. The module which has been added in the process flow consists of conventional Si CMOS process steps (Fig. 2). First, the SOI layer is patterned, encapsulated and doped using boron. Then the encapsulating SiO<sub>2</sub> is partially etched, forming a cavity where the SiO<sub>2</sub> interface, the poly-Si and eventually the Si<sub>0.71</sub>Ge<sub>0.29</sub> layers are deposited. The mono-crystalline Si<sub>0.71</sub>Ge<sub>0.29</sub> alloy is obtained by selective epitaxial growth using Si as seed layer. Accordingly, we then use high temperature SiO<sub>2</sub> deposition for the dielectric interface. Otherwise, in the absence of SiGe, we use rapid thermal oxidation of the SOI layer at temperatures between 850°C and 1050°C to generate the capacitive interface. A thick layer of amorphous Si deposited by LPCVD, followed by a CMP and a crystallisation anneal generates the poly-Si branch of the device [8]. Finally, the poly-Si is patterned and doped by phosphorous implantation. Figure 2b shows a cross-section TEM of the fabricated structure with the relevant BEOL metallization. Further TEM analysis done on dedicated samples also shows the grown SiGe at the capacitive interface (Fig. 2c-d).

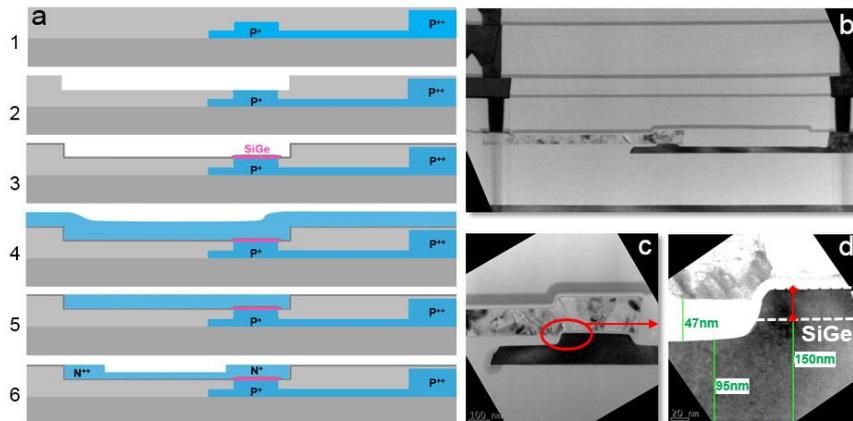


Figure 2: (a) Fabrication steps of the module inserted in the standard flow to generate a capacitive structure. The six main steps consist of a damascene approach to generate the second opto-electrical branch of the device. (b) TEM cross-section showing the patterned capacitive structure and metal interconnections. (c & d) Close-up of the optical section of the device showing both SiGe and oxide interfaces.

### 3. EXPERIMENTAL CHARACTERIZATION

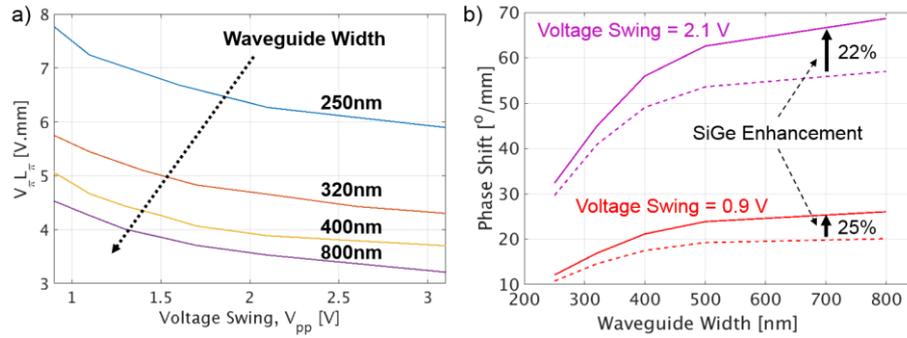


Figure 3: (a) Evolution of  $V_{\pi}L_{\pi}$  for different waveguide widths as a function of the applied voltage. (b) Effect on the phase-shift of a thin SiGe layer above the SOI.

The static features of the modulator are assessed at  $\lambda = 1310\text{nm}$  using  $700\ \mu\text{m}$  phase shifter embedded in a Mach Zehnder interferometer. The modulator efficiency is measured for different waveguide widths ( $W$  on Fig. 1b) at fixed  $t_{\text{ox}} = 7.5\text{nm}$  (Figure 3a). Estimations, using the RC product and the  $V_{\pi}L_{\pi}$  for  $W = 400\text{nm}$  and  $V_{pp} = 0.9\text{V}$  suggest 25 Gbit/s operation feasibility. Such a configuration leads to  $V_{\pi}L_{\pi} = 5\text{V}\cdot\text{mm}$ . Comparatively, this COPA modulator would be 8 times more efficient than a typical pn junction at 25 Gbit/s [1].

SiGe exhibits a stronger electro-optic effect than Si [9]. Modulators with  $t_{\text{ox}} = 13\text{nm}$  and including a 15-nm  $\text{Si}_{0.71}\text{Ge}_{0.29}$  layer below the oxide layer (Fig. 1a) are also characterized (Fig. 4b). The capacitance value is 10% higher as compared with a full Si equivalent structure, while the phase-shift is 25% better (Fig. 3b) but the optical losses are 40% higher. Thus, we observe that the effect of the SiGe layer is significant but not optimized yet. Consequently, we can expect to improve COPA modulators by integrating a well-designed SiGe layer.

### CONCLUSION

We demonstrate the fabrication of a capacitive structure compatible with a full transceiver integration. Experimental characterizations show the high efficiency obtained of the COPA structure, which is 8 times better than using a standard pn-junction. Such a high efficiency allows a reduction of the phase shifter length and required voltage swing which paves the way towards high speed and low power consumption modulators. Furthermore the integration of a SiGe layer below the oxide layer is promising as a 25% improvement of the phase shift has been already obtained

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