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► **To cite this version:**

Lesly-Ann Daniel, Marton Bognar, Job Noorman, Sébastien Bardin, Tamara Rezk, et al.. ProSpeCT: Provably Secure Speculation for the Constant-Time Policy (Extended version). 32nd USENIX Security Symposium, USENIX Security 2023, Aug 2023, Anaheim (CA), United States. 10.48550/arXiv.2302.12108 . hal-04479531

**HAL Id: hal-04479531**

**<https://universite-paris-saclay.hal.science/hal-04479531>**

Submitted on 27 Feb 2024

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# PROSPECT: Provably Secure Speculation for the Constant-Time Policy (Extended version)

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## Abstract

We propose PROSPECT, a generic formal processor model providing provably secure speculation for the constant-time policy. For constant-time programs under a *non-speculative* semantics, PROSPECT guarantees that speculative and out-of-order execution cause no microarchitectural leaks. This guarantee is achieved by tracking secrets in the processor pipeline and ensuring that they do not influence the microarchitectural state during speculative execution. Our formalization covers a broad class of speculation mechanisms, generalizing prior work. As a result, our security proof covers all known Spectre attacks, including load value injection (LVI) attacks.

In addition to the formal model, we provide a prototype hardware implementation of PROSPECT on a RISC-V processor and show evidence of its low impact on hardware cost, performance, and required software changes. In particular, the experimental evaluation confirms our expectation that for a compliant constant-time binary, enabling ProSpeCT incurs no performance overhead.

## 1 Introduction

It is well-understood that microarchitectural optimization techniques commonly used in processors can lead to security vulnerabilities [1]. One of the most recent and challenging problems in this space is the family of Spectre attacks [2], which abuse speculative execution to leak secrets to an attacker that can observe parts of the microarchitectural state of the platform on which the victim is executing.

In response to the discovery of Spectre, a wide range of countermeasures has already been proposed [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. It is an important and difficult challenge to understand the trade-offs offered by these mitigations in terms of security, performance, and applicability to legacy hardware or software.

On the one hand, software countermeasures targeting specific transient execution attacks can still leave other attacks unmitigated [21], and they must be patched every time new

speculation mechanisms are introduced (e.g., the predictive store forwarding feature newly introduced in AMD Zen3 processors [22]). On the other hand, mainstream hardware mitigations have been recently shown ineffective [23] against Spectre-v2 (BTB) attacks [2].

**Hardware-based secure speculation.** In a recent paper, Guarnieri et al. [24] propose *hardware-software contracts* to compare hardware-based mechanisms for secure speculation and better understand how these defenses can enable software to provide end-to-end security guarantees. For instance, they show that certain types of hardware-level taint tracking [12, 16, 18] provide secure speculation for the *sandboxing* policy. On processors implementing one of these mechanisms, the software can simply enforce the sandboxing policy under a non-speculative semantics and does not need to consider the (error-prone and possibly expensive) placement of software speculation barriers.

However, none of the hardware defenses studied under the hardware-software contract framework enable secure speculation for the constant-time policy, except for completely disabling speculative execution. Hence, the classic cryptographic constant-time programming model [25] does not suffice to guarantee security on processors with these countermeasures, and significantly more complex and costly software programming models are required to recover security [21, 26, 27, 28, 29, 30, 31].

**Problem statement.** In this paper, we investigate how to provide efficient provably secure speculation for the constant-time policy under a wide range of speculation mechanisms. Specifically, we apply the hardware-software contract framework to another class of hardware taint-tracking mechanisms explicitly tracking *secrecy* of data in the microarchitecture (e.g., systems like ConTExT [32], SpectreGuard [33], or SPT [34]). In such systems, a constant-time program informs the processor about which memory cells contain secret data. Using this additional information, hardware-based taint-tracking can provide *stronger* security guarantees than sandboxing approaches [24]. Additionally, we consider a wide

variety of speculation mechanisms, whereas the model of Guarnieri et al. considers only speculation on conditional branches.

**Our proposal.** The main contribution of this paper is PROSPECT, a generic processor model formalizing the essence of such secrecy-tracking hardware mechanisms and a proof that it provides secure speculation for the constant-time policy. Specifically, off-the-shelf constant-time cryptographic libraries can be run securely on PROSPECT without additional protections for transient execution attacks.

PROSPECT is modular in the implementation of predictors and covers a broad class of speculation mechanisms, including branch prediction and store-to-load forwarding. As a novel aspect, PROSPECT additionally covers new mechanisms like predictive store forwarding [22] and even mechanisms that are not (yet) implemented in commercial processors, such as load value prediction [35] or value prediction [36]. In particular, we rigorously show that PROSPECT protects against Spectre-v2 (BTB) attacks [2], for which mainstream hardware mitigations have recently been shown ineffective [23]. As evidence for generality, we show that our mechanism even protects against Load Value Injection (LVI) attacks [37], which are particularly challenging to mitigate.

Another novel aspect of our formalization is the statement of our security condition, which allows a program to declassify a ciphertext while still requiring the processor to make sure that the attacker does not learn anything about the plaintext or the key used to compute the ciphertext.

To demonstrate the viability of our proposed mechanism, we extend a RISC-V processor to be PROSPECT-compliant and quantify the hardware costs. Results show that the overhead of PROSPECT in area usage and critical path is reasonable. We also demonstrate that the required software changes to cryptographic code are minimal and that the performance impact is negligible if secrets are precisely annotated. Our prototype is the first non-simulated hardware implementation of a speculative and out-of-order processor that implements secure speculation for the constant-time policy.

**Contribution.** In summary, our contributions are:

- We present PROSPECT, the first formal processor model providing provably secure speculation for the constant-time policy (Section 4). We propose a formal model of a processor that tracks secrets during execution and temporarily blocks speculative execution if secrets could leak. The model is generic; it supports a wide range of speculation mechanisms and formalizes the guarantees provided by prior hardware-based secrecy tracking mechanisms [32, 33, 34].
- We formally prove that PROSPECT provides secure speculation for the constant-time policy, i.e., programs that comply with the classic cryptographic constant-time discipline will not leak secrets through microarchitectural

channels (Theorem 1), including in the presence of declassification (Theorem 2). The proof holds for a large variety of speculation mechanisms, encompassing all known Spectre and LVI attacks.

- We are the first to consider load value speculation. Interestingly, our formal analysis reveals that executions resulting from *correct* load value speculation must sometimes be rolled-back to avoid attacks based on *implicit resolution-based channels* [18]. We prove this formally (Theorem 1) and provide an example in Section 4.6.
- We provide the first non-simulated hardware implementation of a processor offering secure speculation. We implement PROSPECT on a RISC-V processor supporting speculation (Section 6.1) and evaluate the costs of the proposed mechanism in terms of hardware, performance, and manual effort for precisely marking secret data (Section 6.2).

**Availability.** Our implementation and the experimental evaluation are open-sourced at <https://github.com/proteus-core/prospect>.

## 2 Problem statement

### 2.1 Transient execution attacks

Modern processors rely on heavy optimizations to improve performance. They can execute instructions out-of-order to avoid stalling the pipeline when the operands of an instruction are not available. Additionally, they employ *speculation* mechanisms to predict the instruction stream. The execution of instructions resulting from a misprediction, called *transient execution*, is reverted at the architectural level, but effects on the microarchitectural state (e.g., the cache) are persistent.

Spectre attacks [2] exploit these speculation mechanisms to force a victim to leak secrets during transient execution. An attacker can mistrain predictors to force a victim into transiently executing a sequence of instructions, called a Spectre gadget, chosen to encode secrets in the microarchitectural state. Finally, the attacker can use microarchitectural attacks to extract the secret. To this day, many variants of Spectre attacks have been discovered, exploiting a wide variety of speculation mechanisms [2, 3, 22, 38, 39, 40, 41].

Transient execution may also arise from incorrect data being forwarded by faulting instructions. For instance, on some processors, the result of unauthorized loads is transiently forwarded to subsequent instructions before the load is rolled back. This mechanism has first been exploited in Meltdown-style attacks [42, 43] to exfiltrate secret data from another security domain. It is generally accepted that Meltdown-style attacks should be mitigated in hardware by preventing such forwarding from faulting loads. We consider Meltdown-style attacks out of scope for this paper.

However, these faulting loads have also been exploited to *inject* incorrect data into the victim’s transient execution, and, similarly to Spectre attacks, lead the victim to leak their secrets into the microarchitectural state. In particular, these so-called load value injection (LVI) attacks [37] are still possible in the presence of Meltdown mitigations zeroing out the results of faulting loads at the silicon level (i.e., LVI-NULL). LVI attacks are related to Spectre attacks that would exploit *value speculation* during loads.

We illustrate variants of Spectre and LVI attacks in Listing 1, where programs in Listings 1c to 1e abuse different sources of transient execution ( $\mathcal{L}$ ) to encode `SecretVal` in the cache using the `leak` function in Listing 1b. After encoding, the attacker can extract the secret from the cache using cache attacks. Note that while we illustrate these attacks using a cache side-channel, transient execution vulnerabilities are independent of the microarchitectural side-channel they exploit, such as branch predictor state [44], SIMD units [45], port contention [46, 47], micro-op cache [48], etc. Consequently, the `leak(x)` function can be replaced with any other function that reveals information on the value of `x` via a timing or microarchitectural side-channel.

The **Spectre-PHT** (Pattern History Table) or Spectre-v1 variant [2] exploits the conditional branch predictor to transiently execute the wrong side of a conditional branch. For instance, in Listing 1c, an attacker can first mistrain the conditional branch predictor to take the branch and then call the piece of code with `idx = 16` to make the victim transiently execute the branch, accessing `SecretVal` at line 5 and encoding it to the microarchitectural state at line 6.

The **Spectre-BTB** (Branch Target Buffer) or Spectre-v2 variant [2] exploits indirect branch prediction to transiently redirect the control flow to an attacker-chosen location. For example, the program in Listing 1d calls a trusted function, which performs secure computations using `SecretVal`. An attacker can mistrain the branch predictor such that, after line 9, the victim transiently jumps to the `leak` function instead of the trusted function and leaks `SecretVal`. The **Spectre-RSB** (Return Stack Buffer) variant [38, 39] is similar to Spectre-BTB but exploits target predictions for `ret` instructions.

The **Spectre-STL** (Store-To-Load-forwarding) or Spectre-v4 variant [40] exploits the fact that load instructions can speculatively bypass preceding stores. In Listing 1e, the secret located at `ptr_s` is overwritten at line 10, followed by a `load` to the same address, which should return 0. With Spectre-STL, the `load` may bypass the `store` at line 10 and transiently load `SecretVal`, which would then be leaked to the microarchitectural state at line 12.

Finally, **LVI** (Load Value Injection) attacks [37] exploit a faulting `load` to directly inject incorrect data into the victim’s execution. For instance, in Listing 1f, an attacker can prepare the microarchitectural state so that the value 16 is forwarded to `idx` by the `load` instruction at line 13, hence accessing `SecretVal` at line 14 and leaking it at line 15.

## 2.2 Secure speculation approaches

Since transient execution attacks were discovered, several studies have focused on adapting program semantics, security policies, and verification tools to take into account the *speculative semantics* of programs and place extra software-level protections against Spectre attacks, e.g., [21, 28, 29, 30, 31, 49, 50, 51, 52, 53, 54, 55, 56]. However, reasoning about transient execution attacks at the software level only can be burdensome and fragile. Firstly, it necessitates knowledge of microarchitectural details that are often not publicly available. Secondly, it requires changing security policies and applying software patches every time new speculation mechanisms are introduced (e.g., the predictive store forwarding feature newly introduced in AMD Zen3 processors [22]). Finally, software countermeasures targeting specific transient execution attacks can still leave the door open to other attacks [21].

Instead, we argue that, for a given policy  $P$ , enforcement mechanisms at the software level should only consider an architectural (non-speculative) semantics, while the hardware should guarantee that transient execution does not introduce additional vulnerabilities. We call this approach *hardware-based secure speculation for P*.

**Hardware-based secure speculation for sandboxing.** A sandboxing policy isolates a potentially malicious application by restricting the memory range it can access. A program is said to be *sandboxed* if it never accesses memory outside its authorized address range. Sandboxed programs are vulnerable to Spectre attacks, as out-of-bounds memory locations may still be accessed transiently and have their contents leaked to the microarchitectural state. As an example, the program in Listing 1c is sandboxed but can still access and leak out-of-bounds data when the condition is misspeculated.

Some hardware taint-tracking mechanisms [12, 16, 18] have been shown to enable secure speculation for sandboxing [24]. For instance, Speculative Taint Tracking (STT) [18] taints speculatively accessed data and prevents tainted values from being forwarded to instructions that may form a covert channel. In Listing 1c, STT taints the variable `x` at line 5 until the condition at line 4 is resolved. As `x` is tainted, its value is not forwarded to the insecure `load` in the `leak` function.

Unfortunately, hardware-based secure speculation for sandboxing *only protects speculatively accessed data*, meaning that secret data loaded in registers during sequential execution may still be transiently leaked. For instance, STT does not protect the program in Listing 1d against Spectre-BTB. At line 5, a secret is loaded during sequential execution. As a result, `x` is not tainted by STT, and its value can still be forwarded to an insecure instruction if the `jmp` is misspeculated. Hardware-based secure speculation for sandboxing is therefore insufficient to guarantee security for programs that compute on secrets, such as cryptographic primitives. To protect these programs, we need to enable hardware-based secure speculation for the constant-time policy.



```

0 - 15: A[16]
ptr_s (16): SecretVal
17 - 16400: B[256 * 64]

```

(a) Memory

```

1 void leak(x):
2   idx ← x * 64
3   y ← load B + idx ☹

```

(b) Encode x into the cache.

```

4 if (idx < size_A) ℒ
5   x ← load A + idx
6   leak(x)

```

(c) Spectre-PHT (v1)

```

7 f ← trusted_func
8 x ← load ptr_s
9 jmp f(x) ℒ

```

(d) Spectre-BTB (v2)

```

10 store ptr_s 0
11 x ← load ptr_s ℒ
12 leak(x)

```

(e) Spectre-STL (v4)

```

13 idx ← load trusted_idx ℒ
14 x ← load A + idx
15 leak(x)

```

(f) LVI

Listing 1: Examples of code snippets vulnerable to transient execution attacks. The memory layout given in Listing 1a where `SecretVal` is the only secret input and `ptr_s = 16` is common to Listings 1c to 1f. ℒ indicates instructions triggering transient executions and ☹ indicates a leakage.

**Hardware-based secure speculation for constant-time.** A constant-time policy specifies that program secrets should not leak through timing or microarchitectural side channels. Before the advent of transient execution attacks, the constant-time policy was enforced with a coding discipline ensuring that the *control-flow of the program, addresses of memory accesses, and operands of variable-time instructions* do not depend on secret data. This coding discipline is the de facto standard for writing cryptographic code; it has been adopted in many cryptographic libraries [57, 58, 59, 60] and is supported by many tools, e.g., [25, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70].

A standard definition for constant-time programs (i.e., programs adhering to the constant-time policy), and the one we use in this paper, is the following:

**Definition 1** (Constant-time program). A program is constant-time if the observation trace that it produces during *sequential execution* is independent of secret data (where the observation trace records the control flow and memory accesses).<sup>1</sup>

Unfortunately, adhering to this definition is insufficient to guarantee security on modern processors vulnerable to transient execution attacks like Spectre or LVI. Indeed, all programs in Listing 1 are constant-time according to Definition 1, but they are vulnerable to transient execution attacks.

Hardware-based countermeasures guaranteeing secure speculation for sandboxing do not guarantee secure speculation for the constant-time policy. Therefore, to enforce the constant-time policy on speculative processors, it is still necessary to insert specific protections (typically *fence* instructions or *retpolines* [5]) to protect against transient execution attacks. Software developers still have to reason about speculation when they want to enforce the constant-time policy. In this paper, we address the problem of *providing hardware-based provably secure speculation for the constant-time policy*.

<sup>1</sup>We give a formal definition in Section 4.5. For simplicity, we do not include variable-time instructions in our security proofs but discuss how to handle them with PROSPECT.

## 3 Informal overview of PROSPECT

In this section, we motivate our design choices, make explicit what guarantees have to be enforced by software, and sketch the requirements the hardware must enforce. Finally, we illustrate how PROSPECT protects the programs in Listing 1.

### 3.1 Design choices

PROSPECT relies on a hardware-software co-design where developers annotate their secret data, and the hardware guarantees that no information about these secrets can leak during transient execution. The design of PROSPECT is motivated by two main objectives. The first objective is to support existing constant-time code with minimal software changes. To this end, we base our annotation and declassification mechanism on ConTEXT [32] in which developers partition the memory into public and secret regions and can declassify secrets by writing them to public memory. The second objective is to support secure code while maintaining full performance benefits of speculative and out-of-order execution. Specifically, PROSPECT delays speculative execution only when a secret is about to be leaked; hence *in constant-time programs* (which do not leak secrets) PROSPECT *only blocks mispredicted instructions*.

**Software contracts.** Software developers must comply with three contracts:

**Contract 1.** Secret memory locations are labeled.

For instance, in Listing 1, address 16 is labeled as *secret* (or *high*), denoted H, whereas other addresses are labeled as *public* (or *low*), denoted L.

**Contract 2.** The program is constant-time.

**Contract 3.** Secret values written to public memory are *intentionally declassified* by the program.

Contract 3 allows, for instance, cryptographic code to declassify ciphertexts. However, software developers must make sure to not unintentionally declassify secrets by writing them to public memory.

We prove in Section 4.5 that if programs comply with these three contracts, then execution on PROSPECT does not leak secrets through timing and microarchitectural side channels.

**Hardware requirements.** On the hardware side, PROSPECT must realize the following:

**Requirement 1.** During the execution of a program, the processor tracks *security levels*. Concretely, it labels values loaded from memory with their corresponding security level (L or H) and soundly propagates these security levels during computations.

**Requirement 2.** The processor prevents values with security level H to be leaked during speculative execution. Hardware developers identify *insecure instructions* that may leak data through (1) changing the microarchitectural state, (2) influencing the program counter, or (3) exhibiting operand-dependent timing. The processor prevents these instructions from being speculatively executed with secret operands.

**Requirement 3.** Predictions do not leak secret data, in particular: (1) predictor states are only updated using public values, and (2) speculations are rolled back (even the *correct* ones) when their outcome depends on secrets (otherwise, it would leak whether the public prediction is equal to the secret value).

### 3.2 PROSPECT through illustrative examples

Consider the program in Listing 1c, assuming that `idx = 16` and the condition is misspeculated to *true*. When executing the **load** instruction at line 5, PROSPECT tags the register `x` with the security level corresponding to address 16, denoted  $x \mapsto (\text{SecretVal}:\text{H})$  (by Req. 1).<sup>2</sup> Then, when the **leak** function is executed, the **load** instruction (line 3, Listing 1b) is blocked because it would leak a secret-labeled value during speculative execution (by Req. 2). Conversely, if register `x` contains a public-labeled value, i.e.,  $x \mapsto (v:\text{L})$ , the **load** instruction is not blocked. PROSPECT only blocks speculative execution in a few restricted cases, namely when secret data is about to be leaked.

Notice that, contrary to sandboxing-based approaches, PROSPECT also protects secrets loaded in architectural registers from being transiently leaked. For example, in Listing 1d, when the secret is loaded at line 8, `x` is labeled with H, which prevents the secret from being transiently leaked later (by Req. 2) if the **jmp** instruction at line 9 transiently jumps to the **leak** function.

So far, we have seen examples of PROSPECT applied to Spectre-PHT and Spectre-BTB (Spectre-RSB is similar to the latter). The protection generalizes to any other source of speculation, such as load value prediction (which encompasses

<sup>2</sup>A more conservative design choice, adopted by ConTEXT [32], would be to prevent such speculative loads from accessing secret memory locations and to prevent the execution of line 5. However, we formally show that secure speculation is possible with this more liberal design choice.

LVI and Spectre-STL). Take, for instance, the program in Listing 1f. Here, the source of speculation is the **load** instruction, which transiently forwards an incorrect value at line 13. Until the **load** is resolved, PROSPECT considers the following instructions speculative. Consequently, (by Req. 2) it does not forward the secrets to the **load** in the **leak** function (Listing 1b, line 3) and prevents the LVI attack.

Finally, PROSPECT also guarantees (by Req. 3) that predicted values do not depend on secrets. In particular, secret values cannot be speculatively forwarded to other instructions. For example, in Listing 1e, the **load** instruction at line 11 cannot speculatively load `SecretVal`, because the corresponding address is labeled as secret. Notice that PROSPECT still allows forwarding public values.

## 4 Formalization and theorems

This section presents one of the core contributions of this paper, the formalization of PROSPECT. The PROSPECT semantics builds on prior semantics [24], extended to consider a broader spectrum of prediction mechanisms. Moreover, it generalizes the standard constant-time leakage model; in addition to disclosing control-flow and memory accesses, our semantics also discloses *all public-labeled data*. Concretely, all public-labeled data can influence predictions and is observable by an attacker.

### 4.1 ISA language

The ISA is modeled using a small assembly language called  $\mu\text{ASM}$  [29], described in Fig. 1.  $\mathcal{V}$  is a set of values, including memory addresses and program locations, and we let  $v$  and  $l$  range over  $\mathcal{V}$ . `pc` denotes the program counter register, and  $r, x$  denote registers with  $x \neq \text{pc}$ . A program  $P$  is a partial mapping from locations to instructions. We use  $P[l]$  to denote the instruction at location  $l$ .

(Expressions)  $e ::= v \mid r \mid e_1 \otimes e_2$   
(Instructions)  $inst ::= x \leftarrow e \mid \text{jmp } e \mid \text{beqz } e \ l \mid$   
 $x \leftarrow \text{load } e \mid \text{store } e_a \ e_v$

Figure 1: Syntax of  $\mu\text{ASM}$  programs where  $\otimes$  denotes a binary operation.

**Security levels.** We assume a lattice  $\Lambda$  with two security levels: public (low, L) and secret (high, H). We let  $s, s', s_0, \dots$  range over security levels from  $\Lambda$ .  $\sqcup$  denotes the least upper bound operation on the lattice, with  $\text{L} \sqcup \text{H} = \text{H}$ . Additionally, we let  $(v:s)$  denote a value  $v$  with security level  $s$ , ranging over the set  $\hat{\mathcal{V}} = \mathcal{V} \times \Lambda$ . For simplicity, we restrict our description to this 2-level security lattice, but this work generalizes to arbitrary security lattices.

**Location of secret data.** As stated in Contract 1, programmers annotate secret data in the code. In our formal semantics, we assume that they do so by specifying a *security memory partition*  $s_m$ , which maps memory addresses to security levels in  $\Lambda$ . We assume this mapping to be fixed, it cannot change over time. Hence, for the sake of readability, we do not explicitly include it in the configurations of the semantics rules.

## 4.2 Hardware configurations

Hardware configurations are of the form  $\langle m, r, buf, \mu \rangle$ , where  $m$  is the memory, which maps addresses to values in  $\mathcal{V}$ ;  $r$  is the register map, which maps registers to pairs of a value and a security level in  $\hat{\mathcal{V}}$ ;  $buf$  is the reorder buffer, which is a sequence of (possibly transient) instructions; and  $\mu$  is the *microarchitectural context*.

**Microarchitectural context.** The microarchitectural context  $\mu$  can be thought of as the part of the microarchitectural state that the attacker controls. It is an abstract component that models both the *observations* that the attacker can make and the *influence* the attacker has on predictions and scheduling. Formally, it is a stateful deterministic component offering three functions:

- *update*, called by the semantics whenever microarchitectural state possibly leaks to the attacker;
- *predict*, giving the attacker control over predictions, for instance, to predict jump targets or load values;
- *next*, giving the attacker control over scheduling decisions that determine the next processor step to execute.

Hence, our definition of the semantics must make sure that for each computation step,  $\mu$  is updated with all information that could leak from that computation. In particular, updates should include the program counter and the addresses of memory accesses (which *directly* influence the instruction and data cache), but also operands of variable-time instructions (which do not directly influence the microarchitectural state, but might do so *indirectly* via timing variations [71]).

Importantly, to satisfy Req. 2 and 3, our evaluation rules must satisfy the following invariant: if the program is constant-time (as stated in Contract 2), secret data should never leak to  $\mu$ . In particular, the *update* function should never be given secret data as input during speculative execution. It follows from our security theorems that this is indeed the case.

**Reorder buffer.** In out-of-order processors, program instructions are fetched in order and placed in a *reorder buffer* (ROB) where they can be executed out-of-order. Contrary to ISA instructions, ROB instructions, defined in Fig. 2, keep track of the security levels of values. In addition, **jmp** and **beqz** are directly translated to pc assignments when they are fetched and thus are not part of ROB instructions. This also implies that, contrary to ISA instructions, assignments in the ROB

can target pc. Finally, instructions in the ROB with predicted values are tagged with the address  $\mathbb{1}$  of the instruction that the prediction resulted from; otherwise, they are tagged with  $\epsilon$ .

$$\begin{aligned}
 (\text{Tags}) \quad T &::= \mathbb{1} \mid \epsilon \\
 (\text{ROB exp}) \quad e &::= (v:s) \mid r \mid e_1 \otimes e_2 \\
 (\text{ROB inst}) \quad i &::= r \leftarrow e@T \mid x \leftarrow \mathbf{load} \ e@T \mid \\
 &\quad \mathbf{store} \ e_a \ e_v@T
 \end{aligned}$$

Figure 2: ROB instructions.

During the execution, changes that occur in the ROB are applied to the registers using the function *apl* [24]. When the value of an assignment in the reorder buffer is not resolved yet, the corresponding register is mapped to a special symbol  $\perp$ , meaning that it is undefined. Thus, the function *apl* generates a new register map where the value of some registers is undefined.

**Definition 2** (Apply function *apl*). For all register maps  $r$  and reorder buffers  $buf$ :

$$\begin{aligned}
 apl(\epsilon, r) &= r \\
 apl(r \leftarrow (v:s)@T \cdot buf, r) &= apl(buf, r[r \mapsto (v:s)]) \\
 apl(r \leftarrow e@T \cdot buf, r) &= apl(buf, r[r \mapsto \perp]) \text{ if } e \notin \hat{\mathcal{V}} \\
 apl(x \leftarrow \mathbf{load} \ e@T \cdot buf, r) &= apl(buf, r[x \mapsto \perp]) \\
 apl(\mathbf{store} \ e_a \ e_v@T \cdot buf, r) &= apl(buf, r)
 \end{aligned}$$

## 4.3 Sanitization of secret values

An important feature of PROSPECT is the ability to *sanitize* secret values during speculative execution and predictions. To achieve sanitization, we define a low-projection for values denoted  $(v:s)|_L$ . It discloses public values but replaces secret values with  $\perp$ .

**Definition 3** (Low-projection).

$$(v:L)|_L = (v:L) \quad (v:H)|_L = \perp \quad \perp|_L = \perp$$

We let  $r|_L$  be the point-wise extension of  $\cdot|_L$  to register maps. Hence, a sanitized register map  $r|_L$  maps registers to either their value when the associated security level is public or to  $\perp$  when the value is unresolved, or when it is secret.

**Definition 4** (Low memory projection). We define the low-projection of a memory  $m|_L$  such that for all addresses  $a$ :

$$m|_L(a) = \begin{cases} m(a) & \text{if } s_m(a) = L \\ \perp & \text{otherwise} \end{cases}$$

The low-projection of a reorder buffer  $buf$ , denoted  $[buf]|_L$ , discloses all low values in  $buf$ . Values with security level H are replaced by  $\perp$ . On the other hand, values with security level L, unresolved expressions, and tags are not replaced. Details are deferred to Appendix B.

**Sanitizing secrets in speculative execution.** We define a function  $aplsan$  that selectively sanitizes the register map returned by  $apl$ . In sequential execution (i.e., when no instruction in  $buf$  results from a prediction), it directly returns the result of  $apl$ . During speculative execution (i.e., where at least one instruction in  $buf$  results from a prediction), it returns the low-projection of  $apl$ , in which secrets are replaced with  $\perp$ .

**Definition 5** (Apply function  $aplsan(\cdot, \cdot)$ ).

$$aplsan(buf, r) = \begin{cases} apl(buf, r) & \text{if } \forall inst @ T \in buf. T = \epsilon \\ apl(buf, r)|_L & \text{if } \exists inst @ T \in buf. T \neq \epsilon \end{cases}$$

Concretely, the function  $aplsan$  is a crucial part of Req. 2; it acts as a filter that prevents forwarding secret data to insecure instructions (which *update* the microarchitectural context) during speculative execution.

## 4.4 Evaluation rule

**Expression evaluation.** The evaluation of an expression  $e$  with a register map  $r$ , denoted  $\llbracket e \rrbracket_r$ , is a partial function from expressions to labeled values in  $\hat{\mathcal{V}}$ . It is undefined if one of the sub-expressions is undefined. Importantly, the evaluation of a binary operation propagates the security level of its operands in a conservative way (cf. Req. 1); if at least one of the operands has security level H, then the resulting security level is H. Details are available in Appendix B.

**Instruction evaluation.** The hardware semantics is given by a main relation  $c_1 \rightarrow c_2$  and an auxiliary relation  $c_1 \xrightarrow{d} c_2$  where  $c_1$  and  $c_2$  are hardware configurations and  $d$  is a directive. Leaks are **highlighted** in the rules and  $\_$  is used to denote that there exists an expression, but this expression is not important in the context.

The directive determines which processor step to execute: the fetch directive fetches an instruction and places it at the end of the ROB, execute  $i$  executes the  $i^{\text{th}}$  instruction in the ROB, retire removes the oldest instruction from the ROB and commits its changes to the register map and memory.

The STEP rule selects the next directive to apply from the microarchitectural context using the function  $next(\mu)$  and updates the hardware configuration accordingly:

$$\begin{array}{c} \text{STEP} \\ \mu' \triangleq \text{update}(m|_L, r|_L, [buf]_L, \mu) \\ d \triangleq \text{next}(\mu') \quad \langle m, r, buf, \mu' \rangle \xrightarrow{d} \langle m', r', buf', \mu'' \rangle \\ \hline \langle m, r, buf, \mu \rangle \rightarrow \langle m', r', buf', \mu'' \rangle \end{array}$$

The rule updates the microarchitectural context using public-labeled values from the memory  $m|_L$ , the register map  $r|_L$ , and the reorder buffer  $[buf]_L$ . This means that *any public-labeled value can influence subsequent predictions*. In Section 5, we show how this abstraction captures existing prediction mechanisms. It also means that any public-labeled value is leaked

to the attacker, which effectively leaks *more* than the standard constant-time leakage model corresponding to Definition 1.

We present some evaluation rules for each directive, the full set of rules is available in Appendix B.

**Fetch directive.** The instructions are fetched in program order and placed in the ROB. We provide here the rule FETCH-PREDICT-BRANCH-JMP, which applies when the instruction to fetch is a branch or jump.

$$\begin{array}{c} \text{FETCH-PREDICT-BRANCH-JMP} \\ (1; \_ ) \triangleq \llbracket pc \rrbracket_{apl(buf, r)} \\ P[1] \in \{ \mathbf{beqz} \ e \ \_, \ \mathbf{jmp} \ e \} \quad 1' \triangleq \text{predict}(\mu) \\ \langle m, r, buf, \mu \rangle \xrightarrow[\text{fetch}]{} \langle m, r, buf \cdot pc \leftarrow (1'; L) @ 1, \mu \rangle \end{array}$$

The rule predicts the next program location  $1'$  and updates  $pc$  in the ROB accordingly.<sup>3</sup> Notice that the next location  $1'$  is added to the ROB with security level L, hence it will be leaked to the microarchitectural context in the next STEP rule. In the same way, the current location 1, added as a speculation tag in the ROB, is also leaked.

**Execute assignments.** The rule EXECUTE-ASSIGN evaluates an expression  $e$  and updates the value of a register  $r$  in the ROB accordingly. The rule EXECUTE-ASSIGN assumes that the evaluation of the expression  $e$  does not leak information about its operands—in particular, the execution time of the instruction is independent of the value of its operands. In this case, the instruction can securely execute using secret data. Therefore, the rule uses the non-sanitized register map  $apl(buf, r)$  to evaluate  $e$  (cf. the boxed hypothesis). For *variable-time (insecure) instructions* [72, 73, 74], we can simply replace the function  $apl(buf, r)$  in the box with the function  $aplsan(buf, r)$  to prevent the instruction from executing using secret data during speculative execution (cf. Req. 2).

$$\begin{array}{c} \text{EXECUTE-ASSIGN} \\ |buf| = i - 1 \quad e \notin \hat{\mathcal{V}} \quad inst = r \leftarrow e @ T \\ \boxed{(v; s) \triangleq \llbracket e \rrbracket_{apl(buf, r)}} \quad inst' \triangleq r \leftarrow (v; s) @ T \\ \hline \langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot inst' \cdot buf', \mu \rangle \end{array}$$

**Execute loads.** The rule EXECUTE-LOAD-PREDICT predicts the value of a **load** instruction and updates the ROB with this predicted value. Note that the predicted value  $v$  is added to the ROB with security level L and is hence observable. This is consistent with the fact that predictions can only depend on public data (cf. Req. 3).

$$\begin{array}{c} \text{EXECUTE-LOAD-PREDICT} \\ |buf| = i - 1 \\ inst = x \leftarrow \mathbf{load} \ e @ T \quad (1; \_ ) \triangleq \llbracket pc \rrbracket_{apl(buf, r)} \\ v \triangleq \text{predict}(\mu) \quad inst' \triangleq x \leftarrow (v; L) @ 1 \\ \hline \langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot inst' \cdot buf', \mu \rangle \end{array}$$

<sup>3</sup>Note that what we call prediction here also covers store-to-load forwarding, load value prediction, and load value injection, as discussed in Section 5.



The rule EXECUTE-LOAD-COMMIT commits the result of a predicted **load** instruction to the ROB when the prediction is correct. It also leaks the address of the load to the microarchitectural context. The rule uses the *sanitized* value  $a$  of the address, which effectively prevents the rule to be applied during speculative execution when the address is secret (Req. 2). Additionally, notice that the rule can only be applied if the address  $a$  corresponds to public memory (i.e.,  $s_m(a) = L$ ). If the address  $a$  maps to secret memory (meaning that  $m(a)$  is secret), a rollback is performed to prevent leaking whether the secret value  $m(a)$  is equal to the predicted value  $v$ , as described in Req. 3 (a detailed example is provided in Section 4.6).

$$\begin{array}{c} \text{EXECUTE-LOAD-COMMIT} \\ \frac{\begin{array}{l} |buf| = i - 1 \quad inst = x \leftarrow (v:\_)@1_0 \\ P[1_0] = x \leftarrow \mathbf{load} \ e \quad \mathbf{store} \ \_ \notin buf \\ (a:\_) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf,r)} \quad m(a) = v \quad s_m(a) = L \\ inst' = x \leftarrow (v:s_m(a))@e \quad \mu' \triangleq \mathbf{update}(\mu, a) \end{array}}{\langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot inst' \cdot buf', \mu' \rangle}} \end{array}$$

The complementary rule EXECUTE-LOAD-ROLLBACK is applied when the prediction is incorrect or when  $m(a)$  is secret. It commits the correct value to the ROB and drops younger instructions from  $buf'$  (excluding the corresponding pc update).

**Retire directives.** Rules RETIRE-STORE-LOW and RETIRE-STORE-HIGH retire a store instruction on top of the ROB and update the memory accordingly. They also leak the address of the store to the microarchitectural context, following the constant-time leakage model. The rule RETIRE-STORE-LOW is evaluated if the address of the store corresponds to public memory (i.e.,  $s_m(a) = L$ ). In this case, regardless of its original security level, the value  $v$  becomes visible to the attacker: it is *declassified*. As stated in Contract 3, it is the responsibility of the developer to make sure that such declassification is intentional. In Section 4.6, we illustrate declassification in PROSPECT with an example. The declassified value is recorded above the evaluation relation, denoted  $\overset{v}{\rightarrow}$ . It does not affect the semantics but will be used in the theorems of Section 4.5. For secret store locations, the rule RETIRE-STORE-HIGH is applied, which produces an empty declassification trace.

$$\begin{array}{c} \text{RETIRE-STORE-LOW} \\ \frac{\begin{array}{l} buf = \mathbf{store} \ (a:\_) \ (v:\_)@e \cdot buf' \\ \mu' = \mathbf{update}(\mu, a) \quad s_m(a) = L \end{array}}{\langle m, r, buf, \mu \rangle \xrightarrow[\text{retire}]{\overset{v}{\rightarrow}} \langle m[a \mapsto v], r, buf', \mu' \rangle}} \end{array}$$

$$\begin{array}{c} \text{RETIRE-STORE-HIGH} \\ \frac{\begin{array}{l} buf = \mathbf{store} \ (a:\_) \ (v:\_)@e \cdot buf' \\ \mu' = \mathbf{update}(\mu, a) \quad s_m(a) = H \end{array}}{\langle m, r, buf, \mu \rangle \xrightarrow[\text{retire}]{\varepsilon} \langle m[a \mapsto v], r, buf', \mu' \rangle}} \end{array}$$

## 4.5 Theorems

We first define a security theorem for PROSPECT that can be applied to constant-time programs without declassification, and then extend it to capture declassification. The full proofs are available in Appendix E.

An architectural configuration  $\alpha = \langle m, r \rangle$  is the subset of a hardware configuration, consisting of the memory and the register map. The (sequential) architectural semantics is given as a relation  $\alpha \overset{\delta}{\rightsquigarrow}_o \alpha'$ , which evaluates an architectural configuration  $\alpha$  to another architectural configuration  $\alpha'$ . It produces a sequence of observations  $o$  that contains the control flow (changes to the program counter) and the addresses of memory accesses. It also produces a declassification trace  $\delta$ , which is the sequence of all values written to public memory. Evaluation rules are otherwise standard and are provided in Appendix C.

Architectural configurations are said to be *low-equivalent*, written  $\alpha|_L = \alpha'|_L$ , if they are identical in the low-projections of their register maps and memories.

We let  $c_0 \xrightarrow{\delta}^n c_n$  denote an  $n$ -step execution from a hardware configuration  $c_0$  to a configuration  $c_n$ , which produces a *declassification trace*  $\delta$  (details in Appendix B). When  $\delta$  is not needed in the context, it is omitted. Similarly, we let  $\alpha_0 \overset{\delta}{\rightsquigarrow}_o^n \alpha_n$  denote an  $n$ -step execution in the architectural semantics.

**Security for constant-time programs.** PROSPECT guarantees that if a program is constant-time (Contract 2) and does not declassify secret data (Contracts 1 and 3), then it does not leak secret data when running on PROSPECT.

The following definition formalizes the constant-time and no-declassification policy that we expect to be enforced on the software side. In that respect, it establishes a *hardware-software security contract* [24].

**Definition 6** (Constant-time program). A program is constant-time if for any initial architectural configurations  $\alpha_0$  and  $\alpha'_0$  such that  $\alpha_0|_L = \alpha'_0|_L$ , and number of steps  $n$ :

$$\alpha_0 \overset{\delta}{\rightsquigarrow}_o^n \alpha_n \implies \alpha'_0 \overset{\delta'}{\rightsquigarrow}_o^n \alpha'_n \wedge o = o'$$

Additionally, if  $\delta = \delta'$  for all possible  $\alpha_0$  and  $\alpha'_0$ , we say that the program *does not declassify secret data*.

The goal of the attacker is to distinguish two low-equivalent initial configurations  $c$  and  $c'$ , by providing a *strategy*, i.e., a concrete initial microarchitectural context  $\mu_0$  and implementations for *predict*, *update*, and *next* (designed by the attacker to distinguish the configurations). Under any such *deterministic* strategy, the attacker should have the same observations when running in  $c$  and  $c'$ .<sup>4</sup>

<sup>4</sup>Note that nondeterministic strategies would produce different observations due to nondeterminism, not due to differences in secrets being leaked.

**Hypothesis 1.** The functions *predict*, *update*, and *next* are deterministic.

Under this hypothesis, the hardware semantics is deterministic.

The following theorem establishes end-to-end security for constant-time programs without declassification, running on PROSPECT.

**Theorem 1** (Security for constant-time programs.). *For any constant-time program that does not declassify secret data, microarchitectural state  $\mu_0$ , initial configurations  $c_0 = \langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and  $c'_0 = \langle m'_0, r'_0, \varepsilon, \mu_0 \rangle$  such that  $\langle m_0, r_0 \rangle|_L = \langle m'_0, r'_0 \rangle|_L$  and number of steps  $n$ ,*

$$c_0 \rightarrow^n c_n \implies c'_0 \rightarrow^n c'_n \wedge \mu_n = \mu'_n$$

where  $\mu_n$  and  $\mu'_n$  are the microarchitectural contexts in configurations  $c_n$  and  $c'_n$ , respectively.

**Security with declassification.** It is common for cryptographic programs to declassify ciphertexts after an encryption primitive. As we show in Appendix D, classic definitions of declassification [75, 76, 77, 78] allow a program to declassify more information than expected in the context of cryptographic code. Indeed, with such definitions, declassifying  $\mathbb{f}(\mathbb{m})$  implicitly declassifies  $\mathbb{m}$  when  $\mathbb{f}$  is an injective function (e.g., a cryptographic permutation). In contrast, we propose a novel definition of security *up to declassification* that captures the following intuition: if a program only declassifies ciphertexts, then plaintexts and keys remain indistinguishable to an attacker (because they are *cryptographically* indistinguishable) and should not be leaked.

As described above, the declassification trace of an execution  $c \xrightarrow{\delta}^n c'$  is the sequence of all values stored to low (public) memory by the rule RETIRE-STORE-LOW. To express security up to declassification, we introduce a notion of *patched execution*, denoted  $(c, \delta) \hookrightarrow (c', \delta')$ , which replaces values stored to low-memory by values from a declassification trace  $\delta$  (usually obtained by a low-equivalent run in the standard semantics  $\rightarrow$ ). The patched execution ensures that the low-memories of two low-equivalent executions remain equal, achieved by patching the second execution with the declassification trace of the first execution. For instance, a ciphertext that is declassified in the standard semantics can be used to patch another (low-equivalent) execution, to obtain two executions with the same declassified ciphertext (and to make sure that they leak the same values). Concretely, the patched execution only differs from the standard execution by the rule RETIRE-STORE-LOW, which is replaced by the following:

$$\begin{array}{c} \text{RETIRE-STORE-PATCHED} \\ \text{buf} = \text{store}(\mathbf{a}; \_)(\mathbf{v}; \_)\ @ \varepsilon \cdot \text{buf}' \\ \frac{\mu' = \text{update}(\mu, \mathbf{a}) \quad \delta = \mathbf{v}' \cdot \delta' \quad s_m(\mathbf{a}) = \mathbf{L}}{\langle (m, r, \text{buf}, \mu), \delta \rangle \xrightarrow{\text{retire}} \langle (m[\mathbf{a} \mapsto \mathbf{v}'], r, \text{buf}', \mu'), \delta' \rangle} \end{array}$$

We use  $(c, \delta) \hookrightarrow^n (c', \delta')$  to denote the evaluation of  $n$  steps in the patched execution. Similarly, we define a patched execution for the architectural semantics denoted  $(\alpha, \delta) \rightsquigarrow^n (\alpha', \delta')$  and provide the evaluation rules in Appendix C.

**Definition 7** (Constant-time up to declassification). A program is constant-time up to declassification if for any pair of initial architectural configurations  $\alpha_0$  and  $\alpha'_0$  such that  $\alpha_0|_L = \alpha'_0|_L$ , and number of steps  $n$ :

$$\alpha_0 \xrightarrow{\delta}^n \alpha_n \implies (\alpha'_0, \delta) \rightsquigarrow^n (\alpha'_n, \varepsilon) \wedge o = o'$$

The following theorem establishes end-to-end security for constant-time programs up to declassification running on PROSPECT.

**Theorem 2.** *For any constant-time program up to declassification, microarchitectural state  $\mu_0$ , initial configurations  $c_0 = \langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and  $c'_0 = \langle m'_0, r'_0, \varepsilon, \mu_0 \rangle$  such that  $\langle m_0, r_0 \rangle|_L = \langle m'_0, r'_0 \rangle|_L$  and number of steps  $n$ ,*

$$c_0 \xrightarrow{\delta}^n c_n \implies (c'_0, \delta) \hookrightarrow^n (c'_n, \varepsilon) \wedge \mu_n = \mu'_n$$

where  $\mu_n$  and  $\mu'_n$  are the microarchitectural contexts in configurations  $c_n$  and  $c'_n$ , respectively.

In the next section, we provide an example to demonstrate how patched execution works.

## 4.6 Examples

This section showcases key aspects of PROSPECT's semantics through small examples. Example 1 illustrates how declassification works and how PROSPECT prevents forwarding secrets to potential side channels during speculative execution. Example 2 demonstrates that when a predicted load value is resolved and the actual value is secret, speculative execution must be rolled back, even if the prediction was correct.

**Example 1** (Declassification). Consider an execution of the program in Listing 2 (in the standard hardware semantics  $\rightarrow$ ), where the register  $s$  evaluates to  $(s_1; \mathbb{H})$  in the initial configuration. Moreover, we assume that all conditions are predicted to be *true*, but only  $c_1$  can architecturally evaluate to *true*. Under this hypothesis, the program is constant-time up to declassification.

```

1 store a_L f(s) // Declassify f(s)
2 d ← load a_L // Load declassified value
3 if c_1 { x ← load d } // Allowed
4 if c_2 { x ← load s } // Blocked
5 if c_3 { x ← load f(s) } // Blocked

```

Listing 2: Illustration of declassification where  $s$  is a secret input,  $f$  is a one-way function, and  $a_L$  is an address to a public memory location ( $s_m(a_L) = \mathbf{L}$ ). For readability, **beqz** instructions are replaced with **if** constructs.

At line 1, the program computes  $f(s_1)$  and declassifies the result by storing it to public memory. By the rule RETIRE-STORE-LOW, it also produces a declassification trace  $f(s_1)$ .

At line 2, the program loads the declassified value in register  $d$ . By the rule EXECUTE-LOAD-COMMIT,  $d$  has security level  $s_m(a_L) = L$ , hence PROSPECT can speculatively execute the **load** on line 3 to speed up computations before  $c_1$  is resolved. While it speculatively leaks  $d$  to the cache, it is not a security concern because the value has been intentionally declassified (cf. Contract 3).

Notice that because  $f$  is a one-way function, declassifying  $f(s_1)$  does not reveal information about  $s_1$ . In particular, the **load** on line 4 should certainly not be allowed to execute speculatively. PROSPECT faithfully enforces this policy; the rule EXECUTE-LOAD-COMMIT uses *aplsan* to compute the address of the load, and because this happens during speculative execution and  $s$  is labeled secret, we get  $\llbracket s \rrbracket_{aplsan}(buf, r) = \perp$  (cf. Definitions 3 and 5). Hence, the **load** cannot be executed. Similarly, the **load** on line 5 is also blocked because the value  $f(s)$  is recomputed and inherits the secret label from  $s$ .

Now, to illustrate Theorem 2 (security up to declassification), consider a second execution of the program in the *patched semantics* starting with a configuration low-equivalent to the previous one, but where  $s$  evaluates to  $(s_2:H)$  and where declassified values are patched with the declassification trace of the first execution, i.e.,  $f(s_1)$ . According to Theorem 2, the leakage of the first execution and this second patched execution should be the same.

At line 1, the execution evaluates the rule RETIRE-STORE-LOW-PATCHED, which stores the value  $f(s_1)$  at address  $a_L$  (instead of storing  $f(s_2)$ ).

At line 2, the value  $f(s_1)$  is loaded into the register  $d$  and is assigned security level  $s_m(a_L) = L$ .

At line 3 (cf. rule EXECUTE-LOAD-COMMIT), the value of  $d$  can be forwarded to the **load** because its security level is  $L$ . Notice that because the second execution has been patched with the declassification trace of the first execution, the update to the microarchitectural context (i.e., the leakage) is the same in both executions.

At line 4, similarly to the first execution, PROSPECT does not forward the value of  $s$  to the **load** because its security level is  $H$ . By contrast, if we would consider an insecure microarchitecture that forwards the value, the microarchitectural context would be updated with  $s_1$  in the first execution and  $s_2$  in the second execution, which would violate Theorem 2.

Perhaps less intuitively, the leakage at line 5 would also be considered insecure w.r.t. Theorem 2, even though it is semantically equivalent to the leakage at line 3. Indeed, the leakage is not intentional w.r.t. Contract 3, which our security definition takes into account.

In summary, using the notion of *patched execution* allows us to express that there are no microarchitectural leaks be-

yond public information and explicitly declassified values. Even if some other secrets in the program are information-theoretically derivable from declassified values (but, for instance, are cryptographically protected against such derivation), they should still be considered secret. In particular, our declassification condition guarantees that any attack exposing program secrets has to do so based on public information and explicitly declassified values and hence does not rely on any Spectre attack. We believe that for a cryptographic primitive, our definition of declassification can be composed with a standard notion of cryptographic indistinguishability to obtain a stronger notion of cryptographic indistinguishability for the execution of the primitive on PROSPECT.

**Example 2** (Rolling back a correct prediction). Consider the following program, where  $a_H$  is an address to a secret memory location ( $s_m(a_H) = H$ ):

---

```

1 x ← load aH // Load secret value
2 y ← x + 4

```

---

We illustrate step-by-step a (possible) execution flow, focusing on the evolution of *buf* and highlighting **changes** at each step.

- Consider that the scheduler first fetches all instructions:  
 $buf = x \leftarrow \mathbf{load} a_H @ \epsilon \cdot pc \leftarrow (2:L) @ \epsilon \cdot y \leftarrow x + 4 @ \epsilon$
- The scheduler then applies the rule EXECUTE-LOAD-PREDICT and the predictor predicts the loaded value to be 0. Notice that the prediction is public, so we assume that the attacker knows (and can even influence) its value:  
 $buf = x \leftarrow 0 @ 1 \cdot pc \leftarrow (2:L) @ \epsilon \cdot y \leftarrow x + 4 @ \epsilon$
- Next, the scheduler applies the rule EXECUTE-ASSIGN, which computes  $y \leftarrow x + 4$ :  
 $buf = x \leftarrow 0 @ 1 \cdot pc \leftarrow (2:L) @ \epsilon \cdot y \leftarrow 4 @ \epsilon$
- When resolving the prediction, because we have  $s_m(a_H) = H$ , the rule EXECUTE-LOAD-COMMIT cannot be applied, and the execution is rolled back, even if the predicted value (0) was correct:  
 $buf_{rollback} = x \leftarrow 0 @ \epsilon \cdot pc \leftarrow (2:L) @ \epsilon$

Importantly, unconditionally rolling back the execution does not leak information about the secret value  $m(a_H)$ , whereas allowing EXECUTE-LOAD-COMMIT to proceed would leak whether  $m(a_H) = 0$ . Indeed, if  $m(a_H) \neq 0$ , then a rollback would happen, and the final ROB would be  $buf_{rollback}$ . If  $m(a_H) = 0$ , the final ROB would be  $buf_{commit} = x \leftarrow 0 @ \epsilon \cdot pc \leftarrow (2:L) @ \epsilon \cdot y \leftarrow 4 @ \epsilon$ .

Concretely, such a conditional rollback introduces a so-called *implicit resolution-based channel* [18]: the rollback case and the commit case lead to distinct timing behaviors (indeed, contrary to the commit case, the rollback case has to recompute the instructions following the load, which takes extra cycles). While prior solutions [18, 34] address implicit

resolution-based channels (e.g., from memory disambiguation) by delaying the squashing of the implicit branch until prior speculations are resolved, this solution does not apply to load value prediction. Indeed, in our example, the implicit branch is already non-speculative (the processor knows for sure that the value can be committed).

## 5 Discussion

This section discusses prediction mechanisms supported by PROSPECT, limitations, and compatibility with legacy code.

**Prediction mechanisms.** Prior work [18, 79] already stressed the importance of making predictions a function of public data. The novelty of PROSPECT is to allow predictions to depend on *any public data*, hence generalizing standard models of speculative execution. Indeed, public values are used in the STEP rule to update the microarchitectural context  $\mu$ , which is always given as an argument of *predict*. We now discuss how this model encompasses known prediction strategies.

Because the program counter is always public and therefore part of  $\mu$  (cf. Corollary 1 in Appendix E), *predict*( $\mu$ ) always has access to the current (and past) values of the program counter and corresponding instructions. Hence, it can make control-flow predictions based on the full control-flow history, which encompasses existing prediction strategies for conditional branches [80], indirect branches [81], and return targets.

Speculation on memory disambiguation, related to memory-disambiguation machine clears [41] (i.e., Speculative-store-bypass [40] and (predictive) store-to-load-forwarding [22]), is enabled by the rule EXECUTE-LOAD-PREDICT. However, PROSPECT forwards only *public values* from the memory and microarchitectural buffers (the store buffer in particular). This restriction could be lifted by propagating security levels in the store buffer and forwarding predicted values with their security level, as done by SPT [34]. We leave this optimization for future work.

Via the rule EXECUTE-LOAD-PREDICT, our semantics also encompasses the more futuristic load value prediction [35], which can be implemented as forwarding a simple constant or forwarding a value based on the *public* history of load operations. Value prediction [36] (also related to floating-point machine clears [41]), which we do not formalize here for simplicity, is similar to load value prediction. In particular, the prediction should not depend on secrets, and the execution must always be rolled back if the actual value is secret.

Finally, *predict* might also return any arbitrary value, which accounts for predictor states that have been poisoned by an attacker or that forward dummy values, hence encompassing Spectre, as well as LVI (and LVI-NUL) attacks.

**Limitations of PROSPECT.** Memory-ordering machine clears [41] are another source of transient execution, sometimes requiring rolling back memory operations to preserve

memory consistency for concurrent programs. Even though our semantics does not support concurrency, this kind of mechanism could be supported by tracking whether memory instructions might be rolled back w.r.t. to some memory consistency model, similar to speculations. For instance, to support the total-store-ordering model (TSO), the rule EXECUTE-LOAD-COMMIT should additionally make sure that all prior **load** operations in the ROB are resolved (e.g., with an additional hypothesis  $_ \leftarrow \text{load}_ \notin \text{buf}$ ).

Self-modifying code machine clears [41] can also cause transient execution in self-modifying code when the instruction cache (queried in the fetch stage) and the data cache (modified by prior **store** instructions) are desynchronized. Because our semantics assumes instruction memory to be fixed, it does not apply to self-modifying code.

**Legacy software compatibility.** PROSPECT is fully compatible with legacy software. Code without secret annotations works on PROSPECT as is, but without additional security over the base processor. Security and performance can also be traded off: the entire memory (or the stack) can be marked as secret, but it will likely result in additional performance overhead. Finally, to achieve security and optimal performance, only secret-handling code needs to be annotated. For instance, an annotated cryptosystem could be linked securely with (memory-safe) legacy code if the legacy code architecturally accesses only public or declassified information.

## 6 Implementation and evaluation

### 6.1 Implementation

To better understand the costs and benefits of PROSPECT, we built a prototype hardware implementation using the Proteus RISC-V processor framework.<sup>5</sup> Proteus is implemented in SpinalHDL [82], a Scala-based hardware description language (HDL). SpinalHDL generates Verilog or VHDL code that can be run in a simulator or synthesized for an FPGA.

From the many existing open-source RISC-V CPU implementations,<sup>6</sup> we selected Proteus because it is designed to be extended with new hardware mechanisms via a plugin system (inspired by VexRiscv [83]). It is easily configurable in the number of ROB entries and execution units, and it supports branch target prediction and speculative execution, making it vulnerable to Spectre-PHT, -BTB, and -RSB attacks.

PROSPECT is implemented as a Proteus plugin, with some additional modifications in the base processor. In future work, we are looking into combining PROSPECT with other security extensions on Proteus. Our implementation is open-sourced at <https://github.com/proteus-core/prospect>.

**Simplifications.** Our prototype adopts memory partitioning: secrets are co-located in one or more secret memory regions,

<sup>5</sup><https://github.com/proteus-core/proteus>

<sup>6</sup><https://github.com/riscv/riscv-isa-manual/blob/master/marchid.md>



and we manually inform the hardware of the region boundaries. While it is possible to hardcode the boundaries of arbitrary secret regions in hardware, we implemented a more flexible approach that enables the configuration of secret region boundaries via control and status registers (CSRs). The number of CSRs can affect the hardware costs of the implementation; we report on setups allowing one and two secret regions. Note that in our benchmarks, we could co-locate all secrets in a single region when the stack is public and in two regions when the stack is secret. In future work, we plan to develop compiler support for co-locating all secrets in a single region and automatically setting up the secret region boundaries through CSRs.

The prototype takes a conservative approach and stalls every speculative instruction operating on secret data, not only *insecure instructions* (cf. Req. 2). Finally, interrupts are not supported.

**Code size.** The full implementation of a PROSPECT-enabled processor consists of 5275 lines of SpinalHDL code, which generates approximately 104,000 lines of Verilog code. The PROSPECT plugin is written in 90 lines of SpinalHDL, and approximately 270 additional lines of the base Proteus code were modified. For our evaluation, we use 5 execution units and a reorder buffer of size 16. To encourage further experimentation with different configurations, we open-source our evaluation setup.

## 6.2 Evaluation

The security benefit of PROSPECT comes with a tradeoff in three different aspects:

1. *Hardware cost:* PROSPECT uses additional hardware to track secret data and restrict its propagation. This can have an impact on hardware cost metrics like area used and critical path.
2. *Runtime overhead:* PROSPECT can delay the forwarding of secret data, which might impact the execution time of applications.
3. *Labeling of secrets:* Software needs to declare what data is secret, possibly requiring additional developer effort to avoid unintentional declassification (cf. Contract 3).

To validate the security claims of the implementation [84], we executed code samples vulnerable against Spectre on both the base Proteus and the PROSPECT-extended implementation and did not observe leakage in the latter case.

**Hardware cost.** To assess the overhead of the area used and the critical path, we synthesized Proteus without and with the PROSPECT modifications for an Artix-7 XC7A35T FPGA with a speed grade of -1 using Xilinx Vivado. Our experiments showed a reasonable overhead for PROSPECT. The version supporting a single secret region increases the number of slice

LUTs from 16,847 to 19,728 (+17%) and slice registers from 11,913 to 12,600 (+6%). The critical path increases from 30.1 ns to 30.7 ns (+2%). We did not observe any additional increase in these numbers when adding a second set of CSRs to support a second secret region.

**Runtime overhead.** The runtime overhead of PROSPECT depends on two main factors. First, the amount of data marked as secret: if a program only accesses public data, PROSPECT incurs no overhead, while if the whole memory is marked as secret, the overhead is maximal. Second, the performance benefit of speculative execution on the program: if the performance of a program heavily benefits from speculative execution, the overhead of PROSPECT will be higher than if the program does not benefit from speculative execution.

Making a binary PROSPECT-compliant requires co-locating secrets in memory, which could impact performance, e.g. via caching effects. We leave an evaluation of these secondary effects for future work.

Configuring the secret regions from software using CSRs only requires a few additional instructions (loading the boundary addresses into the CSRs before starting the program), resulting in negligible overhead.

We evaluate the first two main factors using the synthetic benchmarks from SpectreGuard [33]. These benchmarks simulate a mix of computations on public data (whose performance heavily benefits from speculative execution) and an encryption routine (whose performance benefits less from speculative execution) with different fractions of speculation/crypto (i.e., S/C). We modify the benchmarks in two ways: (1) because we specifically target constant-time code, we replace the non-constant-time AES primitive with the constant-time `chacha20` primitive from HACL\* [58], (2) we annotate not only the key and plaintext as secret but also all variables that may contain secrets to avoid unintentional declassification (cf. Contract 3).

We ran the benchmarks in three different configurations: the base processor with no PROSPECT extension (our baseline), precisely defining the secret region and defining a secret region to cover the entire address space. More precisely, for the second configuration,  $P(\text{key})$ , we co-locate all secrets in a single region and load the boundaries of this secret region into the CSRs. In the third configuration,  $P(\text{all})$ , we load the first and last address of the memory into the CSRs, protecting the entire address space. Results are given in Table 1, where the percentages denote the relative execution time compared to the baseline for each configuration.

In line with our expectations, our results show that for a PROSPECT-compliant binary, enabling the defense incurs no runtime overhead when secret values are only accessed in constant-time code. When marking the whole memory secret, the overhead ranges from 10% to 45%, which is comparable (but lower) to the overhead of SpectreGuard [33] when

Table 1: Relative SpectreGuard benchmark performance on PROSPECT.

Setting	25S/75C	50S/50C	75S/25C	90S/10C
baseline	100%	100%	100%	100%
$P(\text{key})$	100%	100%	100%	100%
$P(\text{all})$	110%	125%	136%	145%

enabled for the entire address space.<sup>7</sup> Overall, we conclude that PROSPECT incurs a low overhead when secret data is precisely annotated, especially for programs where only a restricted part of the code computes on secrets, which is a common scenario [32, 33] (in SSH clients, web servers, etc.).

**Labeling of secrets.** To benefit from the security guarantees provided by our security theorems, code must be verified to be constant-time in the sequential execution model. Fortunately, verified constant-time implementations of cryptographic primitives are readily available [58], and such verified code also makes explicit what program data should be marked as secret. However, it is still not trivial to identify which memory addresses should be marked as secret. For instance, if the compiler spills secret arguments on the stack, that stack memory must also be marked as secret to avoid unintentional declassification and comply with Contract 3. While it is secure to conservatively over-approximate the memory areas marked as secret (and, for instance, always mark the stack as secret), this has a performance cost.

Hence, we evaluate how difficult it is to obtain precise information about which memory addresses should be labeled secret for a set of representative constant-time cryptographic primitives given in Table 2. To do so, we manually annotate (in the C code) all local variables that may contain secret data, to place them in a dedicated memory section. Additionally, we patch the generated assembly code to clear secret values from registers after declassification. The number of required annotations and assembly lines is reported in Table 2. As a sanity check, we validate that secret data is not written by the compiler to public memory locations outside of the dedicated declassification memory.<sup>8</sup> In the worst case, the time required to annotate secret variables and to validate that no secrets are written on the stack was less than 1 hour.

Interestingly, in 3 of the 4 cryptographic primitives, secret registers are not spilled on the stack by the primitive itself but by the surrounding code. Therefore, for these examples, it is possible to isolate secrets from public data and *keep the stack public* to minimize performance impact.

Finally, for the more complex primitive `curve25519`, secret register spilling cannot easily be avoided manually. Hence, we label the stack as secret, and instead of annotating secret variables, we annotate *public* variables to place them

<sup>7</sup>Of course, no direct comparison can be made as the compiled programs, architectures, and microarchitectures are different.

<sup>8</sup>We track whether secret data is written to non-secret locations using a hardware plugin that we built on top of PROSPECT.

Table 2: Cryptographic primitives used for the experimental evaluation, reporting the lines of C code (LoC), whether the stack (S) is labeled public (L) or secret (H), the number of annotations manually ( $A_m$ ), and automatically ( $A_a$ ) inserted for marking variables, and the number of assembly instructions ( $I$ ) manually inserted.

	LoC	S	$A_m$	$A_a$	$I$	Description
<code>djbssort</code> [85]	246	L	3	0	6	Constant-time sort
<code>sha256</code> [58]	1795	L	34	0	6	Hash function
<code>chacha20</code> [58]	1864	L	51	0	6	Encryption
<code>curve25519</code> [58]	3026	H	9	67	0	Elliptic curve

out of the stack and limit the performance impact. Notice that because the program is constant-time, pointers are public and we can automate their annotation in 67 cases.

In summary, with reasonable manual effort, we were able to keep the stack public for 3 out of 4 cryptographic primitives and isolate public variables from the (secret) stack for the remaining primitive. We expect that this manual effort can easily be automated with compiler support along the lines of existing work for `x86` [32, 86].

## 7 Related work and conclusion

We discussed transient execution attacks throughout the paper, more details can be found in existing surveys [3, 41].

**Formal microarchitectural semantics.** Many studies have proposed operational semantics for speculative execution to formally reason about Spectre attacks (see [87] for a detailed comparison up to 2021). Most previous semantics only capture Spectre-PHT, with a few capturing other variants such as Spectre-STL [21, 27, 28, 88, 89], Spectre-BTB, and Spectre-RSB [27, 28]. Contrary to previous operational semantics, PROSPECT handles *arbitrary* load value prediction [35] and can additionally capture LVI [37]. Using *axiomatic semantics*, Ponce-de-León and Kinder [90] can accommodate new leakage models for different prediction mechanisms and thus cover such cases. In contrast to our work, they can also model attacks based on memory-ordering machine clears [41]. Yet, it is an open question how to model non-interference and declassification, as in our work, using axiomatic semantics.

**Declassification definitions.** Existing leakage models for secure speculation do not permit any kind of leakage [87] that depends on secrets. Yet, in practice, it is common to treat encrypted secrets as observable. In the literature before transient execution attacks, security properties with intentional leakage (i.e., declassification) have been widely studied [91]. When declassifying ciphertexts is a goal, declassification definitions that are not built for this, such as delimited release [76], may consider programs that unintentionally leak secrets (including the cryptographic keys), as secure, as we show in Appendix D. Our definition does not suffer from this limitation and is closer to cryptographically masked flows [92] since it

considers a symbolic model for declassified values. Laud [93] pioneered work in the area of security conditions composable with indistinguishability properties of encryption, which was later generalized to other cryptographic primitives [94, 95]. Later, Laud [96] devised necessary conditions to compose cryptographically masked flows with standard cryptographic indistinguishability properties. We stipulate that our security property will require similar conditions to compose. None of these previous works consider transient execution attacks.

**Hardware defenses against Spectre.** Many defenses specifically target the cache hierarchy [9, 10, 13, 14, 15, 17, 20, 97, 98, 99], yet, these defenses are still vulnerable to attacks exploiting other side channels [44, 45, 46, 47, 48].

Speculative taint-tracking approaches [12, 16, 18, 79] delay instructions that depend on speculatively loaded data. As shown in [24], these approaches enforce hardware-based secure speculation for sandboxing, but offer no protection for non-speculatively accessed data. Hence, they do not provide secure speculation for the constant-time policy.

DOLMA [100] additionally protects non-speculatively accessed data during speculation, but its performance relies on optimizations allowing (under certain conditions) speculative execution of variable-time instructions and memory operations, which might still be exploited via resource contention.

Data oblivious ISA extensions (OISA) [101] are a hardware-based secrecy-tracking mechanism that prevents secret data from leaking, *including during non-speculative execution*. Software must be updated to use the ISA extensions to make sure that secret data is not used as an unsafe operand. In contrast, PROSPECT can be retrofitted into existing ISAs and supports existing (constant-time) cryptographic code with minimal (software and hardware) changes.

**Secure speculation for the constant-time policy.** The idea of propagating security levels from software to hardware and using this information to delay speculative instructions originates from ConTEXT [32] and SpectreGuard [33]. Our work contributes the formalization, security proof, and hardware implementation. While our implementation tracks secret memory regions via CSRs, ConTEXT and SpectreGuard track secrets at a page-level granularity through, for instance, page table entry bits. ConTEXT also tracks public security labels in the cache to reduce over-tainting e.g., when public values are written to the secret stack. As a minor difference, ConTEXT and SpectreGuard completely block the forwarding of secret data during speculative execution, whereas PROSPECT allows executing instructions that do not leak information on their operands. For instance, in the program `if (c) {h ← h + 1}`, if `h` is secret, ConTEXT and SpectreGuard would stall the instruction `h ← h + 1` until speculations are resolved, whereas PROSPECT would allow `h ← h + 1` to speculatively execute. Given a whitelist of secure instructions (e.g., [102]), ConTEXT and SpectreGuard could adopt this less conservative approach while still being secure. Finally, contrary to ConTEXT and SpectreGuard, our

work addresses load value speculation and shows that correct predictions must sometimes be rolled back for security.

Speculative Privacy Tracking (SPT) [34] is another taint-tracking mechanism providing secure speculation for the constant-time policy, but without requiring support from applications. SPT initially considers all data as secret, and whenever a register is architecturally leaked, SPT declassifies (i.e., untaints) the register and propagates the information through the microarchitecture with (forward and backward) untainting. SPT also tracks security labels dynamically in the L1D cache. As an example, consider the program in Listing 3 such that only public values are accessed. When `x1` and `x2` are loaded from memory for the first time, SPT marks them as secret. At line 2, `x1` is architecturally leaked to the microarchitectural state, meaning that it gets untainted. Hence, the `load` at line 4 can be executed speculatively. However, because `x2` is tainted, the `load` at line 5 cannot be executed speculatively. In contrast, on PROSPECT, if the `load` at line 2 corresponds to a public location, then `x2` is set to public and the `load` at line 5 can be executed speculatively. Contrary to SPT, PROSPECT requires annotations but can label data more precisely.

---

```

1  x1 ← load a      // x1:H
2  x2 ← load x1    // x2:H, x1:L
3  if (c) Ⓛ
4      z1 ← load x1 // Continue
5      z2 ← load x2 // Stall

```

---

Listing 3: Taint tracking in SPT where `xi:H` indicates that the register `xi` gets a secret label and `xi:L` indicates that the register `xi` gets untainted.

The above defenses have been implemented in simulators and target the `x86` platform. In contrast, we provide a hardware implementation for RISC-V, which allows us to evaluate hardware costs. PROSPECT generalizes these prior efforts with a formalization supporting a wide range of microarchitectural optimizations capturing recent attacks, and a proof that this enables secure speculation for the constant-time policy.

## Acknowledgments

We are grateful for the valuable feedback of our shepherd and the other reviewers, which helped us improve our paper. This research was partially funded by the ORSHIN project (Horizon Europe grant agreement No. 101070008) and the Flemish Research Programme Cybersecurity. It has also received funding from ANR TAVA, Carnot Flexsecurity, and PEPR Cyber/Secureval.

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## A Artifact Appendix

### A.1 Abstract

The artifact contains the source code of the base Proteus processor extended with PROSPECT, alongside the benchmarks and security tests from our paper. All materials (except for the tool required for hardware cost measurements) are bundled into a Docker container and distributed on GitHub.

### A.2 Description & Requirements

#### A.2.1 Security, privacy, and ethical concerns

None, our artifact is contained in a Docker container, it does not perform any attacks against the host system and it does not use user data.

#### A.2.2 How to access

The artifact is available on GitHub at the following URL: [https://github.com/proteus-core/prospect/tree/usernix\\_artifact](https://github.com/proteus-core/prospect/tree/usernix_artifact).

#### A.2.3 Hardware dependencies

None.

#### A.2.4 Software dependencies

Our artifact uses the following two tools, which are available for both Windows and Linux.

- Docker and 7 GB of disk space for the container (<https://docs.docker.com/engine/install/>).
- Xilinx Vivado 2022.2 Standard Edition, requiring approximately 55 GB of disk space (<https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html>).

#### A.2.5 Benchmarks

Our evaluation uses modified benchmarks from the SpectreGuard paper, which are included in our artifact.

## A.3 Set-up

### A.3.1 Installation

1. Install the two dependencies (Docker and Vivado). Our repository contains detailed instructions on setting up Vivado to minimize the required disk space.
2. Clone our GitHub repository or download the Dockerfile from the root directory ([https://github.com/proteus-core/prospect/tree/usernix\\_artifact](https://github.com/proteus-core/prospect/tree/usernix_artifact)).
3. Build the Docker container by following the instructions in the `README.md` of the repository (building takes approximately 2 hours on a mid-range desktop).

### A.3.2 Basic Test

The security evaluation can be run from the Docker container using the following commands:

```
// first, launch the container  
$ docker run -i -t prospect
```

```
// inside the container, run the tests
```



```
# cd /prospect/tests/spectre-tests/
# ./eval.py /proteus-base/sim/build/base /prospect/sim/build/prospect
TEST secret-before-branch
SECURE VARIANT: Secret did not leak!
INSECURE VARIANT: Secret leaked!
[...]
```

## A.4 Evaluation workflow

### A.4.1 Major Claims

- (C1):** PROSPECT prevents the leakage of secrets from well-annotated programs via Spectre attacks. This is shown by experiment (E1) described in Section 6.2, which executes programs vulnerable to Spectre on the baseline and the extended secure implementation.
- (C2):** PROSPECT incurs no overhead on precisely annotated constant-time code. This is shown by experiment (E2), described in Section 6.2 (Runtime overhead) and Table 1.
- (C3):** PROSPECT only incurs a small overhead in terms of hardware cost. This is shown by experiment (E3), described in Section 6.2 (Hardware cost).

### A.4.2 Experiments

**(E1):** [Security tests, 5 human-minutes]:

**How to:** The experiment is performed in the container by launching a script (identical to the basic test [A.3.2](#)).

**Preparation:** Launch the container with `docker run -i -t prospect` and navigate to the experiment with `cd /prospect/tests/spectre-tests`.

**Execution:** Run the following command:

```
./eval.py /proteus-base/sim/build/base /prospect/sim/build/prospect
```

This will run and evaluate the experiments with both the baseline implementation (first argument) and the PROSPECT-extended version (second argument).

**Results:** The results are displayed as text. The security evaluation should fail with the baseline implementation and succeed with the extension, validating claim (C1).

**(E2):** [Runtime overhead, 5 human-minutes + 9 compute-hours]:

**How to:** The experiment is performed in the container by launching a script.

**Preparation:** Launch the container with `docker run -i -t prospect` and navigate to the experiment with `cd /prospect/tests/synthetic-benchmark`.

**Execution:** Run the following command:

```
./eval.py /proteus-base/sim/build/base_nodump /prospect/sim/build/prospect_nodump
```

This will run and evaluate the experiments with both the baseline implementation (first argument) and the PROSPECT-extended version (second argument), using the variants compiled with no waveform dumping to save disk space.

**Results:** The results are displayed as text. The generated table should reflect Table 1 from the paper, validating claim (C2).

**(E3):** [Hardware cost, 1 human-hour + 2 compute-hours]:

**How to:** The experiment is performed in Vivado, using generated Verilog files from the Docker container.

**Preparation:** Follow the instructions under the heading *Hardware overhead* in `README.md` to obtain the Verilog files used for the synthesis and to set up the Vivado project (*Creating the Vivado project*).

**Execution:** Follow the instructions under the heading *Running the Vivado evaluation* in `README.md` to (iteratively) obtain the hardware costs of both the baseline and the PROSPECT-extended hardware design.

**Results:** The results of the synthesis should be interpreted according to the description under the heading *Interpreting the results* in the `README.md` and compared to the reported numbers in the paper under the heading *Hardware cost* (Section 6.2).

## A.5 Notes on Reusability

Using the `newlib` board support package included in this repository and building on the scripts used for our benchmarks, it is possible to run other benchmarks on Proteus and PROSPECT, making additional benchmarking and security tests possible. The

source code of PROSPECT can also be modified to investigate tradeoffs or to extend the offered security guarantees.

## A.6 Version

Based on the LaTeX template for Artifact Evaluation V20220926. Submission, reviewing and badging methodology followed for the evaluation of this artifact can be found at <https://secartifacts.github.io/usenixsec2023/>.

The appendix includes full rules for the hardware semantics (Appendix B), the architectural semantics (Appendix C), an illustration of why a classical definition of declassification is not strong enough to capture security properties of some cryptographic primitives (Appendix D), and the full proofs of our security theorems (Appendix E).

## B Hardware Semantics

This section provides some details on the hardware semantics that are not crucial for understanding of the main content of the paper, including the definition of initial configurations (Appendix B.1), definition of the low-projection of reorder buffers (Appendix B.2), the full evaluation rules of the hardware semantics (Appendix B.3), the definition of n-step execution (Appendix B.4).

### B.1 Initial configurations

**Definition 8** (Initial configuration). An initial configuration is of the form  $\langle m_0, r_0, buf_0, \mu_0 \rangle$  where  $m_0$  and  $\mu_0$  are arbitrary memory and microarchitectural contexts,  $buf_0$  is empty ( $buf_0 = \varepsilon$ ), and  $r_0$  is a register map such that for all register  $x$ ,  $r(x) \in \hat{\mathcal{V}}$  (i.e., no register maps to  $\perp$ ), and  $r_0(\text{pc}) = (\text{ep:L})$  where  $\text{ep}$  is the entrypoint of the program.

### B.2 Low buffer projection

The low projection of a reorder buffer  $buf$ , discloses all low values in  $buf$ . Values with security level  $L$  are replaced by  $\perp$ . On the contrary, values with security level  $L$ , unresolved expressions, and tags are not replaced.

**Definition 9** (Low buffer projection  $\lfloor buf \rfloor_L$ ). For a reorder buffer  $buf$  its low-projection  $\lfloor buf \rfloor_L$  is given by:

$$\begin{aligned} \lfloor e \rfloor_L &= \begin{cases} \perp & \text{if } e = (v:H) \\ e & \text{otherwise} \end{cases} \\ \lfloor \varepsilon \rfloor_L &= \varepsilon \\ \lfloor r \leftarrow e \rfloor_L &= r \leftarrow \lfloor e \rfloor_L \\ \lfloor x \leftarrow \mathbf{load} e \rfloor_L &= x \leftarrow \mathbf{load} \lfloor e \rfloor_L \\ \lfloor \mathbf{store} e_a e_v \rfloor_L &= \mathbf{store} \lfloor e_a \rfloor_L \lfloor e_v \rfloor_L \\ \lfloor inst @ T \cdot buf \rfloor_L &= \lfloor inst \rfloor_L @ T \cdot \lfloor buf \rfloor_L \end{aligned}$$

### B.3 Full hardware semantics

This section details the evaluation of expressions and the evaluation rules for each directive, `fetch`, `execute`, and `retire`. In this section and in the proof, we mark ROB assignments that increment the program counter as  $\text{pc} \leftarrow^* (v:s)$ , to differentiate them from  $\text{pc}$  assignments resulting from a control-flow instruction (denoted  $\text{pc} \leftarrow (v:s)$ ). This change is purely syntactic and is made to facilitate the proofs; in particular, it does not influence the semantics.

**Expression evaluation** The evaluation of an expression  $e$  with a register map  $r$ , denoted  $\llbracket e \rrbracket_r$ , is given in Fig. 3. It is a partial function from expressions to labeled-values in  $\hat{\mathcal{V}}$ : it is undefined if one of the sub-expressions is undefined ( $r(x) = \perp$ ).

$$\begin{array}{l} \llbracket (v:s) \rrbracket_r = (v:s) \\ \frac{r(x) \in \hat{\mathcal{V}}}{\llbracket x \rrbracket_r = r(x)} \quad \frac{\llbracket e_1 \rrbracket_r = (v_1:s_1) \quad \llbracket e_2 \rrbracket_r = (v_2:s_2)}{\llbracket e_1 \otimes e_2 \rrbracket_r = (v_1 \otimes v_2 : s_1 \sqcup s_2)} \end{array}$$

Figure 3: Evaluation of expressions.

Importantly, the evaluation of a binary operation propagates the security level of its operands in a conservative way (cf. Req. 1): if at least one of the operands has security level H, then the resulting security level is H.

Notice that operations using  $\perp$  operands are undefined which constitutes a side channel that differentiates  $\perp$  from values in  $\hat{\mathcal{V}}$ . However this is not a security concern because it only reveals public information: the security level of operands and whether they are resolved or not. Indeed,  $\perp$  is only introduced in two cases: in the function *aplsan* when the value is marked as secret and is sanitized; and in the function *apl* when an operand is not fully resolved.

### Fetch directive

- **FETCH-PREDICT-BRANCH-JMP** is the evaluation of a **fetch** directive when the instruction to fetch is a branch. The rule predicts the next location  $l'$  and updates `pc` in the ROB accordingly. Notice that the next location  $l'$  is added to the ROB with security level L, hence it will be leaked to the microarchitectural context in the next **STEP** rule. In the same way, the current location  $l$ , which is added as a tag in the ROB is also leaked.
- **FETCH-OTHERS** is the evaluation of a **fetch** directive when the instruction to fetch is not a branch. The rule adds the current instruction to the ROB, increments `pc`,<sup>9</sup> and updates the ROB accordingly. We assume that if the fetched instruction contains an immediate value  $v$ , it is transformed to the ROB expression  $(v:L)$ . Notice that the next location ( $l'$ ) is added to the ROB with security level L, hence it will be leaked to the microarchitectural context in the next **STEP** rule.

$$\begin{array}{c}
\text{FETCH-PREDICT-BRANCH-JMP} \\
\frac{(l:\_)\triangleq \llbracket pc \rrbracket_{apl(buf,r)} \quad P[l] \in \{ \mathbf{beqz} \ e \ \_, \ \mathbf{jmp} \ e \} \quad l' \triangleq \mathit{predict}(\mu)}{\langle m, r, buf, \mu \rangle \xrightarrow{\text{fetch}} \langle m, r, buf \cdot pc \leftarrow (l':L) @ l, \mu \rangle} \\
\\
\text{FETCH-OTHERS} \\
\frac{r' \triangleq \mathit{apl}(buf, r) \quad (l:\_)\triangleq \llbracket pc \rrbracket_{r'} \quad P[l] \notin \{ \mathbf{beqz} \ \_ \ \_, \ \mathbf{jmp} \ \_ \} \quad (l':\_)\triangleq \llbracket pc + 1 \rrbracket_{r'}}{\langle m, r, buf, \mu \rangle \xrightarrow{\text{fetch}} \langle m, r, buf \cdot P[l] @ \varepsilon \cdot pc \leftarrow^* (l':L) @ \varepsilon, \mu \rangle}
\end{array}$$

Figure 4: Evaluation rules for the **FETCH** directive.

### Execute directive for control-flow instructions.

- **BRANCH-COMMIT** (resp. **JMP-COMMIT**) is the execution of a conditional branch (resp. indirect jump) in the ROB. It evaluates the condition (resp. jump target), ensures that the predicted target location  $l$  corresponds to the actual target, and replaces the tag  $l_0$  with  $\varepsilon$  to mark the instruction as resolved.
- **BRANCH-ROLLBACK** (resp. **JMP-ROLLBACK**) is the execution of a conditional branch (resp. indirect jump) in the ROB when the target is incorrectly predicted. The rule discards the instruction that has been mispredicted from the ROB, together with more recent ROB instructions.

### Execute directive for memory and assignments.

- **EXECUTE-ASSIGN** executes an assignment of an expression  $e$  to a register  $r$ . The rule evaluates  $e$  and updates the value of  $r$  in the ROB accordingly.
- **EXECUTE-LOAD-PREDICT** predicts the value of a **load** instruction and updates the ROB accordingly. The prediction is based on the microarchitectural context. Notice that the predicted value  $v$  is added to the ROB with security level L and will therefore be leaked to the microarchitectural context in the **STEP** rule. This is consistent with the fact that predictions only depend on public data.
- **EXECUTE-LOAD-COMMIT** commits the result of a predicted **load** instruction to the ROB. The rule ensures that the ROB does not contain **store** instructions preceding the **load**, evaluates the address  $a$ , retrieves the corresponding value  $m(a)$

<sup>9</sup>For simplicity, we use  $pc + 1$  to denote the increment of the program counter, but the actual expression depends on the architecture. Additionally, it may also depend on the current program location  $P[l]$  without hindering the security guarantees given in Section 4.5.

$$\begin{array}{c}
\text{BRANCH-COMMIT} \\
\frac{|buf| = i - 1 \quad P[1_0] = \mathbf{beqz} \ e \ 1' \quad (c:\_) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf,r)} \quad 1'' \triangleq \text{if } c = 0 \text{ then } 1' \text{ else } 1_0 + 1 \quad 1 = 1''}{\langle m, r, buf \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot pc \leftarrow (1:L) @ \varepsilon \cdot buf', \mu \rangle}
\\
\text{BRANCH-ROLLBACK} \\
\frac{|buf| = i - 1 \quad P[1_0] = \mathbf{beqz} \ e \ 1' \quad (c:\_) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf,r)} \quad 1'' \triangleq \text{if } c = 0 \text{ then } 1' \text{ else } 1_0 + 1 \quad 1 \neq 1''}{\langle m, r, buf \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot pc \leftarrow (1'':L) @ \varepsilon, \mu \rangle}
\\
\text{JMP-COMMIT} \\
\frac{|buf| = i - 1 \quad P[1_0] = \mathbf{jmp} \ e \quad (1':\_) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf,r)} \quad 1' = 1}{\langle m, r, buf \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot pc \leftarrow (1:L) @ \varepsilon \cdot buf', \mu \rangle}
\\
\text{JMP-ROLLBACK} \\
\frac{|buf| = i - 1 \quad P[1_0] = \mathbf{jmp} \ e \quad (1':\_) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf,r)} \quad 1' \neq 1}{\langle m, r, buf \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf', \mu \rangle \xrightarrow[\text{execute } i]{} \langle m, r, buf \cdot pc \leftarrow (1'':L) @ \varepsilon, \mu \rangle}
\end{array}$$

Figure 5: Evaluation rules for the EXECUTE directive (for control-flow instructions).

from the memory, determines the corresponding security level  $s_m(a)$ , and updates the ROB. The rule also leaks the value of the index to the microarchitectural context. Notice that the rule can only be applied if the address  $a$  corresponds to public memory ( $s_m(a) = L$ ). If the address  $a$  maps to secret memory (meaning that  $m(a)$  is secret), the EXECUTE-LOAD-ROLLBACK is executed instead, in order to prevent leaking whether the secret value  $m(a)$  is equal to the predicted value  $v$ .

- EXECUTE-LOAD-ROLLBACK discards the result of a predicted **load** instruction from the ROB. Similarly to EXECUTE-LOAD-COMMIT, the rule computes the address and value of the **load**. Contrary to EXECUTE-LOAD-COMMIT, the predicted value  $v$  is replaced by the actual value  $m(a)$  and younger instructions in the ROB are discarded (excluding the corresponding  $pc$  update). Notice that the rule is applied if the **load** value has been mispredicted or if it is secret.
- EXECUTE-STORE evaluates both operands of a store instruction and adds the result to the reorder buffer. Notice that the value of the store is not yet committed to the memory (it will be committed in the rule RETIRE-STORE). However, if its security level is public, it can be used to the update microarchitectural context in the STEP rule. In particular, it means that a store value can be forwarded to a load instruction, only if it is public.

### Retire directive.

- RETIRE-ASSIGN retires an assignment on top of the ROB and updates the register map accordingly;
- RETIRE-STORE and RETIRE-STORE-DECL retire a store instruction on top of the ROB and updates the memory accordingly. These rules also updates the microarchitectural context with the index of the store. The rule RETIRE-STORE-DECL is applied when a secret is declassified, meaning that the value is marked as secret while the address of the store corresponds to a part of the memory that is observable by the attacker (i.e.,  $s_m(a) = \perp$ ). In this case, the value  $v$  becomes visible to the attacker (i.e., it is declassified). The rule also produces a declassification trace with the declassified value  $v$ ;
- RETIRE-PATCHED replaces the rule RETIRE-STORE-DECL in the patched semantics. Similarly to the rule RETIRE-STORE-DECL, it is applied when a secret is declassified. It replaces the value that is declassified with a value from a declassification trace  $\delta$ .

## B.4 n-step execution

A  $n$ -step execution in the hardware semantics, denoted  $c \xrightarrow{\delta}^n c'$ , makes  $n$  evaluation steps from a configuration  $c$  to a configuration  $c'$ . Additionally, it produces a *declassification trace*  $\delta$  that is the sequence of declassified values:



$$\begin{array}{c}
\text{EXECUTE-ASSIGN} \\
\frac{|buf| = i - 1 \quad e \notin \hat{\mathcal{V}} \quad inst = r \leftarrow e @ T \quad \boxed{(v:s) \triangleq \llbracket e \rrbracket_{apl(buf,r)}} \quad inst' \triangleq r \leftarrow (v:s) @ T}{\langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow{\text{execute } i} \langle m, r, buf \cdot inst' \cdot buf', \mu \rangle} \\
\\
\text{EXECUTE-LOAD-PREDICT} \\
\frac{|buf| = i - 1 \quad inst = x \leftarrow \mathbf{load} e @ T \quad (l:_ ) \triangleq \llbracket pc \rrbracket_{apl(buf,r)} \quad v \triangleq \text{predict}(\mu) \quad inst' \triangleq x \leftarrow (v:L) @ 1}{\langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow{\text{execute } i} \langle m, r, buf \cdot inst' \cdot buf', \mu \rangle} \\
\\
\text{EXECUTE-LOAD-COMMIT} \\
\frac{|buf| = i - 1 \quad inst = x \leftarrow (v:_ ) @ 1_0 \quad P[1_0] = x \leftarrow \mathbf{load} e \quad \mathbf{store} \_ \_ \notin buf \\ (a:_ ) \triangleq \llbracket e \rrbracket_{aplsan(buf,r)} \quad m(a) = v \quad s_m(a) = L \quad inst' = x \leftarrow (v:s_m(a)) @ \varepsilon \quad \mu' \triangleq \text{update}(\mu, a)}{\langle m, r, buf \cdot inst \cdot buf', \mu \rangle \xrightarrow{\text{execute } i} \langle m, r, buf \cdot inst' \cdot buf', \mu' \rangle} \\
\\
\text{EXECUTE-LOAD-ROLLBACK} \\
\frac{|buf| = i - 1 \quad inst = x \leftarrow (v:_ ) @ 1_0 \quad P[1_0] = x \leftarrow \mathbf{load} e \quad \mathbf{store} \_ \_ \notin buf \\ (a:_ ) \triangleq \llbracket e \rrbracket_{aplsan(buf,r)} \quad m(a) \neq v \vee s_m(a) = H \quad inst' = x \leftarrow (m(a):s_m(a)) @ \varepsilon \quad \mu' \triangleq \text{update}(\mu, a)}{\langle m, r, buf \cdot inst \cdot pc \leftarrow^* (l:s) @ \varepsilon \cdot buf', \mu \rangle \xrightarrow{\text{execute } i} \langle m, r, buf \cdot inst' \cdot pc \leftarrow^* (l:s) @ \varepsilon, \mu' \rangle} \\
\\
\text{EXECUTE-STORE} \\
\frac{|buf| = i - 1 \quad e_a, e_v \notin \hat{\mathcal{V}} \quad (a:_ ) \triangleq \llbracket e_a \rrbracket_{aplsan(buf,r)} \quad \boxed{(v:s) \triangleq \llbracket e_v \rrbracket_{apl(buf,r)}}}{\langle m, r, buf \cdot \mathbf{store} e_a e_v @ T \cdot buf', \mu \rangle \xrightarrow{\text{execute } i} \langle m, r, buf \cdot \mathbf{store} (a:L) (v:s) @ T \cdot buf', \mu \rangle}
\end{array}$$

Figure 6: Evaluation rules for the EXECUTE directive (assignment and memory instructions).

**Definition 10** ( $n$ -step execution). For any microarchitectural configuration  $c$ :

$$c \xrightarrow{\varepsilon}^0 c \qquad \frac{c \xrightarrow{\delta}^{n-1} c'' \quad c'' \xrightarrow{v} c'}{c \xrightarrow{\delta \cdot v}^n c'}$$

A  $n$ -step patched execution, denoted  $(c, \delta) \hookrightarrow^n (c', \delta')$  is defined as follows:

**Definition 11** ( $n$ -step patched execution). For any microarchitectural configuration  $c$ :

$$(c, \delta) \hookrightarrow^0 (c, \delta) \qquad \frac{(c, \delta) \hookrightarrow^{n-1} (c'', \delta'') \quad (c'', \delta'') \hookrightarrow (c', \delta')}{(c, \delta) \hookrightarrow^n (c', \delta')}$$

$$\begin{array}{c}
\text{RETIRE-ASSIGN} \\
\frac{buf = r \leftarrow (v:s) @ \varepsilon \cdot buf'}{\langle m, r, buf, \mu \rangle \xrightarrow[\text{retire}]{} \langle m, r[r \mapsto (v:s)], buf', \mu \rangle} \\
\\
\text{RETIRE-STORE-LOW} \\
\frac{buf = \mathbf{store} (a:_) (v:_) @ \varepsilon \cdot buf' \quad \mu' = \text{update}(\mu, a) \quad s_m(a) = L}{\langle m, r, buf, \mu \rangle \xrightarrow[\text{retire}]{} \langle m[a \mapsto v], r, buf', \mu' \rangle} \\
\\
\text{RETIRE-STORE-HIGH} \\
\frac{buf = \mathbf{store} (a:_) (v:_) @ \varepsilon \cdot buf' \quad \mu' = \text{update}(\mu, a) \quad s_m(a) = H}{\langle m, r, buf, \mu \rangle \xrightarrow[\text{retire}]{} \langle m[a \mapsto v], r, buf', \mu' \rangle} \\
\\
\text{RETIRE-STORE-PATCHED} \\
\frac{buf = \mathbf{store} (a:_) (v:_) @ \varepsilon \cdot buf' \quad \mu' = \text{update}(\mu, a) \quad \delta = v' \cdot \delta' \quad s_m(a) = L}{\langle m, r, buf, \mu \rangle, \delta \xrightarrow[\text{retire}]{} \langle m[a \mapsto v'], r, buf', \mu' \rangle, \delta'}
\end{array}$$

Figure 7: Evaluation rules for the RETIRE directive.

## C Architectural Semantics

This section defines the architectural semantics, including the definition of architectural configurations (Appendix C.1), the full evaluation rules (Appendix C.2), and the definition of n-step executions (Appendix C.3).

### C.1 Architectural configurations

The sequential execution operates on *architectural configurations*  $\langle m, r \rangle$  where  $m$  and  $r$  are a memory and a register map, similar to hardware configurations. Notice that even though register maps keep track of the taint of registers, the sequential semantics simply ignores the taint. Therefore, we write  $r(x) = v$  instead of  $r(x) = (v:s)$  when  $s$  is not needed.

**Definition 12** (Initial configuration). An initial configuration is of the form  $\langle m_0, r_0 \rangle$  where  $m_0$  is an arbitrary memory, and  $r_0$  is a register map such that for all register  $x$ ,  $r_0(x) \in \hat{\mathcal{V}}$  (i.e., no register maps to  $\perp$ ), and  $r_0(\text{pc}) = (\text{ep:L})$  where  $\text{ep}$  is the entrypoint of the program.

Notice that for any initial architectural configuration  $\langle m_0, r_0 \rangle$ , and microarchitectural context  $\mu_0$ ,  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle$  is also an initial hardware configuration as defined in Definition 8.

### C.2 Full evaluation rules of the architectural semantics

The architectural semantics is given by a relation  $\langle m, r \rangle \xrightarrow[\delta]{o} \langle m', r' \rangle$  which evaluates an instruction in a configuration  $\langle m, r \rangle$  to a configuration  $\langle m', r' \rangle$  and produces an observation  $o$  and a declassification trace  $\delta$ . When the declassification trace is empty, it is omitted. The rules are given in Fig. 8.

The leakage model that we consider in sequential semantics corresponds to the standard constant-time leakage model [25, 57, 103]. In particular, the rule BRANCH leaks the outcome of the condition, the rule JMP leaks the jump target, the rule LOAD and STORE leak the memory address that is accessed. The STORE rule additionally produces a declassification trace when writing to the low part of the memory (i.e.,  $s_m(a) = L$ ).

Additionally, to express security with declassification in a similar way as for the hardware semantics, we define a patched architectural semantics, denoted  $\langle m, r \rangle, \delta \xrightarrow{\delta'} \langle m', r' \rangle, \delta'$ . The patched architectural semantics is similar to the sequential semantics given in Fig. 8 but replaces the STORE rule with the rules STORE-HIGH and STORE-PATCHED given in Fig. 9. The rule STORE-HIGH applies when the store address corresponds to the secret part of the memory and behaves like a standard store. The rule STORE-PATCHED applies when the store address corresponds to the public part of memory and replaces the value with a value from the declassification trace  $\delta$ .

### C.3 n-step execution

A  $n$ -step execution in the architectural semantics, denoted  $\alpha \xrightarrow[\delta]{o}^n \alpha'$ , makes  $n$  evaluation steps from a configuration  $\alpha$  to a configuration  $\alpha'$ . It produces a *observation trace*  $o$  that is the sequence of individual observations produced by each rule, and a

$$\begin{array}{c}
\text{BRANCH} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = \mathbf{beqz} \ e \ 1' \quad c \triangleq \llbracket e \rrbracket_r \quad 1'' \triangleq \text{if } c = 0 \text{ then } 1' \text{ else } 1 + 1}{\langle m, r \rangle \xrightarrow[c=0]{\sim} \langle m, r[\text{pc} \mapsto 1''] \rangle} \\
\\
\begin{array}{cc}
\text{JMP} & \text{ASSIGN} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = \mathbf{jmp} \ e \quad 1' \triangleq \llbracket e \rrbracket_r}{\langle m, r \rangle \xrightarrow[1]{\sim} \langle m, r[\text{pc} \mapsto 1'] \rangle} & \frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = x \leftarrow e \quad v \triangleq \llbracket e \rrbracket_r}{\langle m, r \rangle \xrightarrow[\varepsilon]{\sim} \langle m, r[\text{pc} \mapsto 1 + 1][x \mapsto v] \rangle}
\end{array} \\
\\
\text{LOAD} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = x \leftarrow \mathbf{load} \ e \quad a \triangleq \llbracket e \rrbracket_r \quad v \triangleq m(a)}{\langle m, r \rangle \xrightarrow[a]{\sim} \langle m, r[\text{pc} \mapsto 1 + 1][x \mapsto v] \rangle} \\
\\
\text{STORE} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = \mathbf{store} \ e_a \ e_v \quad a \triangleq \llbracket e_a \rrbracket_r \quad v \triangleq \llbracket e_v \rrbracket_r \quad \delta \triangleq \text{if } s_m(a) = L \text{ then } v \text{ else } \varepsilon}{\langle m, r \rangle \xrightarrow[a]{\delta} \langle m[a \mapsto v], r[\text{pc} \mapsto 1 + 1] \rangle}
\end{array}$$

Figure 8: Evaluation rules of the architectural semantics.

$$\begin{array}{c}
\text{STORE-HIGH} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = \mathbf{store} \ e_a \ e_v \quad a \triangleq \llbracket e_a \rrbracket_r \quad v \triangleq \llbracket e_v \rrbracket_r \quad s_m(a) = H}{\langle m, r \rangle, \delta \xrightarrow[a]{\sim} \langle m[a \mapsto v], r[\text{pc} \mapsto 1 + 1] \rangle, \delta} \\
\\
\text{STORE-PATCHED} \\
\frac{1 \triangleq \llbracket \text{pc} \rrbracket_r \quad P[1] = \mathbf{store} \ e_a \ e_v \quad a \triangleq \llbracket e_a \rrbracket_r \quad s_m(a) = L \quad \delta = v \cdot \delta'}{\langle m, r \rangle, \delta \xrightarrow[a]{\sim} \langle m[a \mapsto v], r[\text{pc} \mapsto 1 + 1] \rangle, \delta'}
\end{array}$$

Figure 9: Evaluation rules of the patched architectural semantics.

declassification trace  $\delta$  that is the sequence of declassified values:

**Definition 13** ( $n$ -step execution). For any architectural configuration  $\alpha$ :

$$\alpha \xrightarrow[\varepsilon]{\sim}^0 \alpha \quad \frac{\alpha \xrightarrow[o]{\delta}^{n-1} \alpha'' \quad \alpha'' \xrightarrow[o']{v} \alpha'}{\alpha \xrightarrow[o \cdot o']{\delta \cdot v}^n \alpha'}$$

A  $n$ -step patched execution, denoted  $(\alpha, \delta) \xrightarrow[o]{\sim}^n (\alpha', \delta')$  is defined as follows:

**Definition 14** ( $n$ -step patched execution). For any architectural configuration  $\alpha$ :

$$(\alpha, \delta) \xrightarrow[\varepsilon]{\sim}^0 (\alpha, \delta) \quad \frac{(\alpha, \delta) \xrightarrow[o]{\sim}^{n-1} (\alpha'', \delta'') \quad (\alpha'', \delta'') \xrightarrow[o']{\sim} (\alpha', \delta')}{(\alpha, \delta) \xrightarrow[o \cdot o']{\sim}^n (\alpha', \delta')}$$

## D Problem with Classical Declassification

Classic definitions of declassification require the absence of leakage for pairs of executions agreeing on their declassification traces [75, 76, 77, 78]:

**Theorem 3.** *For all constant-time program  $P$ , number of steps  $n$ , memories  $m_0, m'_0$ , register maps  $r_0, r'_0$ , and microarchitectural state  $\mu_0$ ,*

$$m_0|_L = m'_0|_L \wedge r_0|_L = r'_0|_L \wedge \langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta}^n \langle m_n, r_n, buf_n, \mu_n \rangle \implies \\ \langle m'_0, r'_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta'}^n \langle m'_n, r'_n, buf'_n, \mu'_n \rangle \wedge (\delta = \delta' \implies \mu_n = \mu'_n)$$

**Problem** The problem with Theorem 3 is that it allows for declassifying more information than intended. For instance, declassifying the output of a one-way function  $f(m)$ , does not reveal information on the secret  $m$ . Consequently, it should not be allowed to leak the value of  $m$  because  $f(m)$  has been declassified. In Example 3, we show that the notion of declassification given in Theorem 3 fails to capture this intuition and that declassifying  $f(m)$  can also implicitly declassify  $m$ .

**Example 3.** Consider the execution of the program in Listing 4 from two low-equivalent initial configuration with respective secret input  $r(m) = (m_1:H)$  and  $r'(m) = (m_2:H)$  on an insecure speculative out-of-order processor.

At line 1, the first execution declassifies  $f(m_1)$  and the second execution declassifies  $f(m_2)$ . Consider that the code at line 2 is speculatively executed. In this case  $m_1$  and  $m_2$  are leaked during speculative execution in the first and second executions respectively. Notice that because  $f$  is a one-way function, declassifying the value of  $f(m)$  does not give away information on the value of  $m$ . Therefore, the program should be considered insecure.

However, because Listing 4 restricts to pairs of traces with the same declassification trace, it only check the absence of leakage under the condition  $f(m_1) = f(m_2)$ . Under this condition, we have  $m_1 = m_2$  because  $f$  is injective. Consequently, these executions satisfy Theorem 3. In other words, declassifying  $f(m)$  also implicitly declassifies  $m$ .

---

```

1 store aL f(m) // Declassify f(m)
2 if v1 { load m } // Leak secret m

```

---

Listing 4: Illustration of declassification where  $m$  is a secret input,  $f$  is a injective one-way function, and  $a_L$  is an address to a public memory location.

Notice that PROSPECT, provides stronger guarantees than what is captured by Theorem 3. Because  $m$  is labeled as secret, it is not forwarded to the speculative **load** at line 2 and cannot be speculatively leaked. As a consequence, we need an alternative definition of declassification that captures more complex notions of security relevant to cryptographic primitives.



## E Proofs

The architectural semantics, together with our definition of constant-time programs can be thought of as a hardware-software security contract, similar to contracts proposed in prior work [24]. Hence, our proofs naturally builds on the proofs given in prior work [24] that relate security contracts to hardware semantics, in particular Appendix E.1 and Appendix E.1. The former establishes a correspondence relation between the architectural semantics and the hardware semantics, and the latter establishes a correspondence relation between the patched architectural semantics and the patched hardware semantics. The main adaptations are related to the load value speculation and the patched semantics. Appendix E.2 establishes some useful lemmas to reason about low-equivalent pairs of executions. Appendix E.3 contains the proof for our security theorem applicable to constant-time programs *without* declassification (cf. Theorem 1), and Appendix E.5 contains the proof for our security theorem applicable to constant-time programs *with* declassification (cf. Theorem 2).

### E.1 Correspondence between architectural and hardware semantics

**Notations** We let  $buf[i]$  with  $0 \leq i \leq |buf|$  denote the  $i^{th}$  instruction in the reorder buffer  $buf$  and let  $buf[0] = \varepsilon$ . Additionally, we let  $buf[i..j]$  with  $0 \leq i \leq j \leq |buf|$  be the restriction of the buffer  $buf$  to instructions between  $i$  and  $j$  (included). We let  $\vec{\alpha}$  (resp.  $\vec{c}$ ) denote a sequence of architectural configuration or (resp. hardware configuration) resulting from a execution in the architectural (resp. hardware) semantics. Given a sequence of architectural configurations  $\vec{\alpha}$ , we let  $\alpha_j$  with  $0 \leq j < |\vec{\alpha}|$  denote the  $j^{th}$  configuration in  $\vec{\alpha}$  (the same holds for  $\vec{c}$ ).

The following lemma directly follows from the syntax of the ISA language (cf. Fig. 1).

**Lemma 1.** *A program does not modify its control-flow with direct assignments to  $pc$ .*

The deep update of an architectural configuration  $\langle m, r \rangle$  with a reorder buffer  $buf$ , denoted  $\langle m, r \rangle \uplus \varepsilon$ , applies all pending instructions in  $buf$  to the configuration  $\langle m, r \rangle$ . Notice that predicted values in  $buf$  are first resolved to their correct value before being applied.

**Definition 15** (Deep update). For any reorder buffer  $buf$  and architectural configuration  $\langle m, r \rangle$ :

$$\begin{aligned}
 \langle m, r \rangle \uplus \varepsilon &\triangleq \langle m, r \rangle \\
 \langle m, r \rangle \uplus_{x \leftarrow e} e @ T &\triangleq \begin{cases} \langle m, r[x \mapsto \llbracket e \rrbracket_r] \rangle & \text{if } T = \varepsilon \\ \langle m, r[x \mapsto (m(\llbracket e_a \rrbracket_r) : sm[\llbracket e_a \rrbracket_r])] \rangle & \text{if } T = 1 \wedge P[1] = x \leftarrow \mathbf{load} \ e_a \end{cases} \\
 \langle m, r \rangle \uplus_{pc \leftarrow e} e @ T &\triangleq \begin{cases} \langle m, r[pc \mapsto \llbracket e \rrbracket_r] \rangle & \text{if } T = \varepsilon \\ \langle m, r[pc \mapsto \llbracket e_l \rrbracket_r] \rangle & \text{if } T = 1 \wedge P[1] = \mathbf{jump} \ e_l \\ \langle m, r[pc \mapsto 1'] \rangle & \text{if } T = 1 \wedge P[1] = \mathbf{beqz} \ e_c \ 1' \wedge \llbracket e_c \rrbracket_r = 0 \\ \langle m, r[pc \mapsto 1 + 1] \rangle & \text{if } T = 1 \wedge P[1] = \mathbf{beqz} \ e_c \ 1' \wedge \llbracket e_c \rrbracket_r \neq 0 \end{cases} \\
 \langle m, r \rangle \uplus_{x \leftarrow \mathbf{load} \ e_a} e_a @ T &\triangleq \langle m, r[x \mapsto (m(\llbracket e_a \rrbracket_r) : sm[\llbracket e_a \rrbracket_r])] \rangle \\
 \langle m, r \rangle \uplus \mathbf{store} \ e_a \ e_v @ T &\triangleq \langle m[\llbracket e_a \rrbracket_r \mapsto \llbracket e_v \rrbracket_r], r \rangle \\
 \langle m, r \rangle \uplus (inst @ T \cdot buf) &\triangleq (\langle m, r \rangle \uplus inst @ T) \uplus buf
 \end{aligned}$$

The predicate  $wf(buf, \langle m, r \rangle)$  defines what it means for a reorder buffer  $buf$  to be well-formed with respect to a configuration  $\langle m, r \rangle$ .

**Definition 16** (Well-formed reorder-buffers). A reorder buffer  $buf$  is well-formed for an architectural configuration  $\langle m, r \rangle$  the

following conditions hold:

$$\begin{aligned}
& wf(\varepsilon, \langle m, r \rangle) \\
& wf(inst \cdot buf, \langle m, r \rangle) \text{ if } wf(inst, \langle m, r \rangle) \wedge wf(buf, \langle m, r \rangle) \uplus inst \\
& wf(p_c \leftarrow (1:L)@ \varepsilon, \langle m, r \rangle) \text{ if } P[\llbracket p_c \rrbracket_r] \in \{ \mathbf{beqz} \ x \ l', \ \mathbf{jmp} \ e \} \\
& wf(p_c \leftarrow (1:L)@ 1_0, \langle m, r \rangle) \text{ if } \llbracket p_c \rrbracket_r = 1_0 \wedge P[1_0] \in \{ \mathbf{beqz} \ x \ l', \ \mathbf{jmp} \ e \} \\
& wf(p_c \xleftarrow{*} (1:L)@ \varepsilon, \langle m, r \rangle) \\
& wf(x \leftarrow e @ \varepsilon \cdot p_c \xleftarrow{*} (1:L)@ \varepsilon, \langle m, r \rangle) \text{ if } P[\llbracket p_c \rrbracket_r] \in \{ x \leftarrow e, x \leftarrow \mathbf{load} \ e \} \wedge 1 = P[\llbracket p_c + 1 \rrbracket_r] \\
& wf(x \leftarrow (v:L)@ 1_0 \cdot p_c \xleftarrow{*} (1:L)@ \varepsilon, \langle m, r \rangle) \text{ if } \llbracket p_c \rrbracket_r = 1_0 \wedge P[1_0] = x \leftarrow \mathbf{load} \ e \wedge 1 = P[\llbracket p_c + 1 \rrbracket_r] \\
& wf(x \leftarrow \mathbf{load} \ e @ \varepsilon \cdot p_c \xleftarrow{*} (1:s)@ \varepsilon, \langle m, r \rangle) \text{ if } P[\llbracket p_c \rrbracket_r] = x \leftarrow \mathbf{load} \ e \wedge 1 = P[\llbracket p_c + 1 \rrbracket_r] \\
& wf(\mathbf{store} \ e_a \ e_v @ \varepsilon \cdot p_c \xleftarrow{*} (1:s)@ \varepsilon, \langle m, r \rangle) \text{ if } P[\llbracket p_c \rrbracket_r] = \mathbf{store} \ e_a \ e_v \wedge 1 = P[\llbracket p_c + 1 \rrbracket_r] \wedge e_a, e_v \notin \hat{\mathcal{V}} \\
& wf(\mathbf{store} \ (a:L) \ (v:s) @ \varepsilon \cdot p_c \xleftarrow{*} (1:s)@ \varepsilon, \langle m, r \rangle) \text{ if } P[\llbracket p_c \rrbracket_r] = \mathbf{store} \ e_a \ e_v \wedge 1 = P[\llbracket p_c + 1 \rrbracket_r] \wedge a = \llbracket e_a \rrbracket_r \wedge v = \llbracket e_v \rrbracket_r
\end{aligned}$$

The following lemma states that hardware executions produce well-formed reorder buffers.

**Lemma 2** (Reorder-buffers are well-formed). *For any initial configuration  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and number of steps  $n$  such that  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle \rightarrow^n \langle m_n, r_n, buf_n, \mu_n \rangle$ , then  $wf(buf_n, \langle m_n, r_n \rangle)$ .*

*Proof.* The proof goes by induction on the number of steps and case analysis on the evaluation rules of the hardware semantics.  $\square$

It follows, that at any point of the execution  $p_c$  is always defined and its security level is always L.

**Corollary 1** (Security level of  $p_c$  is L). *For all initial configuration  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and number of steps  $n$ , such that  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle \rightarrow^n \langle m_n, r_n, buf_n, \mu_n \rangle$ , then:*

$$r_n(p_c) = (\_ : L) \text{ and } p_c \leftarrow e @ T \in buf_n \implies e = (\_ : L) \quad (1)$$

*Proof.* The proof follows from the fact that reorder-buffers are well-formed (cf. Lemma 2), and well-formed buffers only contain resolved assignments to  $p_c$  with security level L (cf. Definition 16).

Additionally,  $p_c$  is initially set to security level L in the register map and is only updated with well-formed ROB assignments.  $\square$

The following lemma expresses that undefined values are never committed to the register map.

**Lemma 3** (Well defined architectural register maps). *For all initial configuration  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and number of steps  $n$  such that  $\langle m_0, r_0, \varepsilon, \mu_0 \rangle \rightarrow^n \langle m_n, r_n, buf_n, \mu_n \rangle$ , then for all register  $\tau$ ,  $r_n(\tau) \in \hat{\mathcal{V}}$ .*

*Proof.* The proof goes by induction on the number of steps. The base case follows from Definition 8. The inductive case follows from the instruction evaluation rules. In particular the rule RETIRE-ASSIGN is the only rule that modifies the register map and only updates the mapping of a register with a value in  $\hat{\mathcal{V}}$ .  $\square$

The following predicates define what it means for a hardware configuration  $c$  to be transient, denoted  $transient(c)$ , and what it means for a ROB instruction  $inst @ \varepsilon$ , to be correctly predicted with respect to a configuration  $\langle m, r \rangle$ , denoted  $goodpred(inst @ \varepsilon, \langle m, r \rangle)$ .

**Definition 17** (Transient ROB). For all hardware configuration  $\langle m, r, buf, \_ \rangle$ , and architectural configuration  $\langle m, r \rangle$ :

$$transient(\langle m, r, buf, \_ \rangle) \triangleq \begin{cases} false & \text{if } \forall 1 \leq i \leq |buf|. goodpred(buf[i], \langle m, r \rangle \uplus buf[0..i-1]) \\ true & \text{otherwise} \end{cases}$$

$$goodpred(inst @ \varepsilon, \langle m, r \rangle)$$

$$goodpred(pc \leftarrow (1:\_) @ 1_0, \langle m, r \rangle) \text{ if } P[1_0] = \mathbf{beqz} \ e \ 1' \wedge \llbracket e \rrbracket_r = 0 \wedge 1 = 1'$$

$$goodpred(pc \leftarrow (1:\_) @ 1_0, \langle m, r \rangle) \text{ if } P[1_0] = \mathbf{beqz} \ e \ 1' \wedge \llbracket e \rrbracket_r \neq 0 \wedge 1 = 1_0 + 1$$

$$goodpred(pc \leftarrow (1:\_) @ 1_0, \langle m, r \rangle) \text{ if } P[1_0] = \mathbf{jmp} \ e \wedge \llbracket e \rrbracket_r = 1$$

$$goodpred(x \leftarrow (v:\_) @ 1_0, \langle m, r \rangle) \text{ if } P[1_0] = x \leftarrow \mathbf{load} \ e \wedge \llbracket e \rrbracket_r = a \wedge s_m(a) = L \wedge m(a) = v$$

The prefixes of a reorder buffer  $buf$  with respect to a configuration  $\langle m, r \rangle$ , denoted  $prefix(buf, \langle m, r \rangle)$ . Notice that the prefixes of a ROB only contain correctly predicted sequences of instructions with respect to  $\langle m, r \rangle$ . If  $buf$  contains a transient instructions it will be included as the last instruction of the longest prefix but subsequent instructions will not be included.

**Definition 18** (Prefix of reorder buffer). For a configuration  $\langle m, r \rangle$  and well-formed reorder buffer  $buf$ ,  $prefix(buf, \langle m, r \rangle)$  is defined as:

$$prefix(\varepsilon, \langle m, r \rangle) \triangleq \{\varepsilon\}$$

$$prefix(pc \leftarrow (1:s) @ \varepsilon \cdot buf, \langle m, r \rangle) \triangleq \{\varepsilon\} \cup \{pc \leftarrow (1:s) @ \varepsilon \cdot buf' \mid buf' \in prefix(buf, \langle m, r \rangle) \uplus pc \leftarrow (1:s) @ \varepsilon\}$$

$$prefix(pc \leftarrow (1:s) @ 1_0 \cdot buf, \langle m, r \rangle) \triangleq \{\varepsilon, pc \leftarrow (1:s) @ 1_0\} \cup \{pc \leftarrow (1:s) @ 1_0 \cdot buf' \mid$$

$$buf' \in prefix(buf, \langle m, r \rangle) \uplus pc \leftarrow (1:s) @ 1_0 \wedge goodpred(pc \leftarrow (1:s), 1_0, \langle m, r \rangle)\}$$

$$prefix(inst @ \varepsilon \cdot pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf, \langle m, r \rangle) \triangleq \{\varepsilon\} \cup \{inst @ \varepsilon \cdot pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf' \mid buf' \in prefix(buf, \langle m, r \rangle) \uplus inst @ \varepsilon \cdot pc \xleftarrow{*} (1:s) @ \varepsilon\}$$

$$prefix(inst @ 1_0 \cdot pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf, \langle m, r \rangle) \triangleq \{\varepsilon, inst @ 1_0 \cdot pc \xleftarrow{*} (1:s) @ \varepsilon\} \cup \{inst @ 1_0 \cdot pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf' \mid$$

$$buf' \in prefix(buf, \langle m, r \rangle) \uplus inst @ 1_0 \cdot pc \xleftarrow{*} (1:s) @ \varepsilon \wedge goodpred(inst @ 1_0, \langle m, r \rangle)\}$$

$$prefix(pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf, \langle m, r \rangle) \triangleq \{pc \xleftarrow{*} (1:s) @ \varepsilon\} \cup \{pc \xleftarrow{*} (1:s) @ \varepsilon \cdot buf' \mid buf' \in prefix(buf, \langle m, r \rangle) \uplus pc \xleftarrow{*} (1:s) @ \varepsilon\}$$

where  $inst \notin \{pc \leftarrow e, pc \xleftarrow{*} e\}$ .

Given a contract run  $\vec{\alpha}$  and a hardware run  $\vec{c}$ , the correspondence relation  $corr_{\vec{\alpha}, \vec{c}}$  maps prefixes of reorder buffers of hardware states in  $\vec{c}$  to their corresponding architectural states in  $\vec{\alpha}$ . In particular,  $corr_{\vec{\alpha}, \vec{c}}(n)(i) = j$  indicates that the prefix of length  $i$  of  $buf_n$  corresponds to the architectural state  $\alpha_j$  (where  $buf_n$  denotes the ROB in the  $n^{th}$  hardware state in  $\vec{c}$  and  $\alpha_j$  denoted the  $j^{th}$  architectural state in  $\vec{\alpha}$ ).

**Definition 19** (Correspondence relation). Let  $\alpha_0 = \langle m, r \rangle$  be an initial architectural configuration and  $\mu$  be a microarchitectural context. Additionally, let  $\vec{\alpha}$  be the longest contract run, starting from  $\alpha_0$ , and  $\vec{c}$  be the longest PROSPECT run starting from  $c_0 = \langle m, r, \varepsilon, \mu \rangle$ . Additionally, for all  $0 \leq n < |\vec{c}|$ , we let  $c_n$  denote the  $n^{th}$  configuration in  $\vec{c}$ .

The correspondence relation  $corr_{\vec{\alpha}, \vec{c}}$  is defined as follows:

$$corr_{\vec{\alpha}, \vec{c}}(0) \triangleq \{0 \mapsto 0\}$$

$$corr_{\vec{\alpha}, \vec{c}}(n) \triangleq \begin{cases} fetch_{\vec{\alpha}, \vec{c}}(n) & \text{if } next'(c_{n-1}) = fetch \wedge \neg transient(c_{n-1}) \\ corr_{\vec{\alpha}, \vec{c}}(n-1) & \text{if } next'(c_{n-1}) = fetch \wedge transient(c_{n-1}) \\ corr_{\vec{\alpha}, \vec{c}}(n-1) & \text{if } next'(c_{n-1}) = execute \ i \wedge \neg transient(c_{n-1}) \\ shift(corr_{\vec{\alpha}, \vec{c}}(n-1)) & \text{if } next'(c_{n-1}) = retire \wedge \neg transient(c_{n-1}) \end{cases}$$

where

$$fetch_{\vec{\alpha}, \vec{c}}(n) \triangleq \begin{cases} corr_{\vec{\alpha}, \vec{c}}(n-1)[|buf_{n-1}| + 1 \mapsto corr_{\vec{\alpha}, \vec{c}}(n-1)(|buf_{n-1}| + 1)] & \text{if } P[lst\_pc(c_{n-1})] \in \{\mathbf{beqz} \ \_, \mathbf{jmp} \ \_\} \\ corr_{\vec{\alpha}, \vec{c}}(n-1)[|buf_{n-1}| + 2 \mapsto corr_{\vec{\alpha}, \vec{c}}(n-1)(|buf_{n-1}| + 1)] & \text{if } P[lst\_pc(c_{n-1})] \notin \{\mathbf{beqz} \ \_, \mathbf{jmp} \ \_\} \end{cases}$$

$$shift(map) \triangleq \lambda i \in \mathbb{N}. map(i+1)$$

$$next'(\langle m, r, buf, \mu \rangle) \triangleq next(update(m|_L, r|_L, [buf]_L, \mu))$$

$$lst\_pc(\langle m, r, buf, \mu \rangle) \triangleq r'(pc) \text{ where } \langle \_, r' \rangle = \langle m, r \rangle \uplus buf$$

The following lemma states that for all non-transient buffer  $buf$  with respect to a configuration  $\langle m, r \rangle$ , the register map obtained by the function  $apl$  is equivalent (when defined) to the register map obtained by the deep update of  $buf$  with  $\langle m, r \rangle$ .

**Lemma 4.** *Let  $\langle m, r \rangle$  be an architectural configuration and  $buf$  a reorder buffer such that  $\neg\text{transient}(\langle m, r, buf, \_ \rangle)$ . Let  $\langle \_, r' \rangle = \langle m, r \rangle \uplus buf$ . We have that for all  $x$  if  $apl(buf, r)(x) = (v:s)$  then  $r'(x) = (v:s)$ .*

*Proof.* The proof goes by induction on the size of the ROB, Definition 2 and Definition 15. In particular, the following cases require particular attention:

For the case  $inst = pc \leftarrow 1@T$ , because we have  $\neg\text{transient}(\langle m, r, buf, \_ \rangle)$ , then  $\langle m, r \rangle \uplus pc \leftarrow 1@T = \langle m, r[pc \mapsto 1] \rangle$ . Additionally, we also have  $apl(pc \leftarrow 1@T) = r[pc \mapsto 1]$ . Hence applying  $inst$  with  $apl$  or  $\uplus$  gives the same register map.

For the case  $inst = x \leftarrow \mathbf{load} e_a@T$ , we get with  $apl$  that  $x$  is undefined, which immediately concludes our goal.

For the case  $inst = \mathbf{store} e_a e_v@T$ , the instruction is ignored by  $apl$  but the memory is modified in  $\uplus$ . Note that it only impacts the result of subsequent  $inst = x \leftarrow \mathbf{load} e@T$  instructions but these instructions result in undefined  $x$  with  $apl$ , which immediately concludes our goal.  $\square$

**Corollary 2.** *Let  $\langle m, r \rangle$  be an architectural configuration and  $buf$  a reorder buffer such that  $\neg\text{transient}(\langle m, r, buf, \_ \rangle)$ . Let  $\langle \_, r' \rangle = \langle m, r \rangle \uplus buf$ . We have that for all expression  $e$ ,  $\llbracket e \rrbracket_{apl(buf, r)} = (v:\_)$  then  $\llbracket e \rrbracket_{r'} = (v:\_)$ .*

*Proof.* This follows directly from Lemma 4 and by structural induction on the expression evaluation (cf. Fig. 3).  $\square$

**Corollary 3.** *Let  $\langle m, r \rangle$  be an architectural configuration and  $buf$  a reorder buffer such that  $\neg\text{transient}(\langle m, r, buf, \_ \rangle)$ . Let  $\langle \_, r' \rangle = \langle m, r \rangle \uplus buf$ . We have that for all expression  $e$ ,  $\llbracket e \rrbracket_{aplsan(buf, r)} = (v:\_)$  then  $\llbracket e \rrbracket_{r'} = (v:\_)$ .*

*Proof.* Observe by definition of  $aplsan$  (cf. Definition 5), that  $\llbracket e \rrbracket_{aplsan(buf, r)} = (v:\_) \implies \llbracket e \rrbracket_{apl(buf, r)} = (v:\_)$ . Form there,  $\llbracket e \rrbracket_{r'} = (v:\_)$  follows directly by application of Corollary 2.  $\square$

The following lemma states that for each hardware state in an hardware run, for all the prefixes of its reorder buffer, there exists a corresponding architectural state in the corresponding architectural run.

**Lemma 5** (Correctness of the  $\text{corr}_{\vec{\alpha}, \vec{c}}$  relation). *Let  $\alpha_0 = \langle m, r \rangle$  be an initial architectural configuration and  $\mu$  be a microarchitectural context. Additionally, let  $\vec{\alpha}$  be the longest contract run, starting from  $\alpha_0$ , and  $\vec{c}$  be the longest PROSPECT run starting from  $c_0 = \langle m, r, \varepsilon, \mu \rangle$ . Additionally, for all  $0 \leq n < |\vec{c}|$ , we let  $c_n$  denote the  $n^{\text{th}}$  configuration in  $\vec{c}$ .*

*For all  $0 \leq n < |\vec{c}|$ , we have:*

$$\text{For all } buf \in \text{prefix}(buf_n, \langle m_n, r_n \rangle), \langle m_n, r_n \rangle \uplus buf = \alpha_j \text{ where } j = \text{corr}_{\vec{\alpha}, \vec{c}}(n)(|buf|). \quad (\text{G})$$

*Proof.* The proof goes by induction on  $n$ .

**Base case** ( $n = 0$ ). We have  $c_0 = \langle m, r, \varepsilon, \mu \rangle$ , hence  $buf_0 = \varepsilon$ . From Definition 18, we have that  $\text{prefix}(\varepsilon) = \{\varepsilon\}$ . Additionally, from Definition 19, we have that  $j = \text{corr}_{\vec{\alpha}, \vec{c}}(0)(|\varepsilon|) = 0$ . From Definition 15, we have that  $\langle m, r \rangle \uplus \varepsilon = \langle m, r \rangle = \alpha_0$ , which concludes (G).

**Inductive case.** Assume that the hypothesis holds for hardware runs of length  $n - 1$ , namely:

$$\text{For all } buf \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle), \langle m_{n-1}, r_{n-1} \rangle \uplus buf = \alpha_j \text{ where } j = \text{corr}_{\vec{\alpha}, \vec{c}}(n-1)(|buf|). \quad (\text{IH})$$

We show that (G) holds at step  $n$ , more precisely after taking a step  $c_{n-1} \rightarrow c_n$ , (G) holds for the configuration  $c_n$ .

First, notice that  $c_n$  is obtained by application of the STEP rule, which applies the directive  $d \triangleq \text{next}'(c_{n-1})$ . Hence the proof follows by case analysis on the directive  $d$ .

**Fetch directive.** When  $d = \text{fetch}$ , two rules may apply: FETCH-PREDICT-BRANCH-JMP and FETCH-PREDICT-OTHERS. We consider both cases separately.

FETCH-PREDICT-BRANCH-JMP: from the hardware evaluation rules (cf. Fig. 4), we have  $buf_n = buf_{n-1} \cdot pc \leftarrow (1':L)@1$  where  $(1:\_)$   $\triangleq \llbracket pc \rrbracket_{apl(buf_{n-1}, r_{n-1})}$ , and  $P[1] \in \{\mathbf{beqz} \_ \_, \mathbf{jmp} \_ \_ \}$ . Additionally, we have  $m_n = m_{n-1}$  and  $r_n = r_{n-1}$ . We have to consider two cases:

- *transient*( $c_{n-1}$ ). From Definition 19, we have that  $\text{corr}_{\vec{\alpha}, \vec{c}}(n) = \text{corr}_{\vec{\alpha}, \vec{c}}(n-1)$ . Additionally, from Definition 18, because there is a transient instruction in  $buf_{n-1}$  and because  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , we have  $\text{prefix}(buf_n, \langle m_n, r_n \rangle) = \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . From there, (G) directly follows from (IH).



- $\neg\text{transient}(c_{n-1})$ . Because  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , we have  $\text{prefix}(buf_n, \langle m_n, r_n \rangle) = \text{prefix}(buf_n, \langle m_{n-1}, r_{n-1} \rangle)$ . From this, Definition 18, the definition of  $buf_n$  and the fact that  $buf_n$  is well formed (from Lemma 2), we get

$$\text{prefix}(buf_n, \langle m_n, r_n \rangle) = \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle) \cup \{buf_n\}$$

Let  $buf$  be an arbitrary prefix in  $\text{prefix}(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

1.  $buf \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . From (IH) and  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , we have  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(|buf|)}$ . Moreover, from Definition 19 and because  $|buf| \leq |buf_{i+1}|$ , we have  $\text{corr}_{\bar{\alpha}, \bar{c}}(n)(|buf|) = \text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(|buf|)$ , which entails  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\bar{\alpha}, \bar{c}}(n)(|buf|)}$  and concludes (G) for this case.
2.  $buf \notin \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ , in which case  $buf = buf_n = buf_{n-1} \cdot \text{pc} \leftarrow (1':L)@1$ . Because  $\neg\text{transient}(c_{n-1})$  and because reorder buffers are well-formed (Lemma 2), we have from Definition 18 that  $buf_{n-1} \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have

$$\langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1} = \alpha_j \text{ where } j = \text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(|buf_{n-1}|)$$

In the following, we let  $\alpha_j = \langle r_j, m_j \rangle$ . From Corollary 2 and  $(1':L) = \llbracket \text{pc} \rrbracket_{\text{apl}(buf_{n-1}, r_{n-1})}$ , we have  $r_j(\text{pc}) = (1':L)$  and hence  $\text{Ist\_pc}(c_{n-1}) = 1$ , which means  $P[\text{Ist\_pc}(c_{n-1})] \in \{\mathbf{beqz\_}, \mathbf{jmp\_}\}$ . From this, Definition 19, and  $|buf| = |buf_{n-1}| + 1$ , we get  $\text{corr}_{\bar{\alpha}, \bar{c}}(n)(|buf|) = \text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(|buf_{n-1}|) + 1 = j + 1$ .

Additionally, from Definition 15, we have that  $\langle m_n, r_n \rangle \uplus buf = (\langle m_n, r_n \rangle \uplus buf_{n-1}) \uplus \text{pc} \leftarrow (1':L)@1$ . From  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , and the definition of  $\alpha_j$ , this gives us  $\langle m_n, r_n \rangle \uplus buf = \alpha_j \uplus \text{pc} \leftarrow (1':L)@1$ . Hence, in order to show  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\bar{\alpha}, \bar{c}}(n)(|buf|)}$  (which concludes our goal (G) for this case), it remains to show

$$\alpha_j \uplus \text{pc} \leftarrow (1':L)@1 = \alpha_{j+1}$$

From there, we have to consider several cases:

- (a)  $P[1] = \mathbf{beqz} e \text{ l}_{\text{br}}$  and  $\llbracket e \rrbracket_{r_j} = 0$ . In this case, from Definition 15, we have  $\alpha_j \uplus \text{pc} \leftarrow (1':L)@1 = \langle m_j, r_j[\text{pc} \mapsto \text{l}_{\text{br}}] \rangle$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 8, rule BRANCH), we also have  $\alpha_{j+1} = \langle m_j, r_j[\text{pc} \mapsto \text{l}_{\text{br}}] \rangle$ , which concludes  $\alpha_j \uplus \text{pc} \leftarrow (1':L)@1 = \alpha_{j+1}$ .
- (b)  $P[1] = \mathbf{beqz} e \text{ l}_{\text{br}}$  and  $\llbracket e \rrbracket_{r_j} \neq 0$ . In this case, from Definition 15, we have  $\alpha_j \uplus \text{pc} \leftarrow (1:L)@1 = \langle m_j, r_j[\text{pc} \mapsto 1 + 1] \rangle$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 8, rule BRANCH), we also have  $\alpha_{j+1} = \langle m_j, r_j[\text{pc} \mapsto 1 + 1] \rangle$ , which concludes  $\alpha_j \uplus \text{pc} \leftarrow (1':L)@1 = \alpha_{j+1}$ .
- (c)  $P[1] = \mathbf{jmp} e$ . In this case, from Definition 15, we have  $\alpha_j \uplus \text{pc} \leftarrow (1:L)@1 = \langle m_j, r_j[\text{pc} \mapsto \llbracket e \rrbracket_{r_j}] \rangle$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 8, rule JMP), we also have  $\alpha_{j+1} = \langle m_j, r_j[\text{pc} \mapsto \llbracket e \rrbracket_{r_j}] \rangle$ , which concludes  $\alpha_j \uplus \text{pc} \leftarrow (1':L)@1 = \alpha_{j+1}$ .

We have shown that for an arbitrary  $buf \in \text{prefix}(buf_n, \langle m_n, r_n \rangle)$  we have  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\bar{\alpha}, \bar{c}}(n)(|buf|)}$ , which concludes (G).

FETCH-OTHERS: from the hardware evaluation rules (cf. Fig. 4), we have  $buf_n = buf_{n-1} \cdot \text{inst} @ \varepsilon \cdot \text{pc} \leftarrow (1 + 1:L)@ \varepsilon$  where  $(1':L) \triangleq \llbracket \text{pc} \rrbracket_{\text{apl}(buf_{n-1}, r_{n-1})}$ ,  $\text{inst} = P[1]$  and  $\text{inst} \notin \{\mathbf{beqz\_}, \mathbf{jmp\_}\}$ . Additionally, we have  $m_n = m_{n-1}$  and  $r_n = r_{n-1}$ . We have to consider two cases:

- $\text{transient}(c_{n-1})$ . The proof is similar to the case FETCH-PREDICT-BRANCH-JMP.
- Because  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , we have  $\text{prefix}(buf_n, \langle m_n, r_n \rangle) = \text{prefix}(buf_n, \langle m_{n-1}, r_{n-1} \rangle)$ . From this, Definition 18, the definition of  $buf_n$  and the fact that  $buf_n$  is well formed (from Lemma 2), we get

$$\text{prefix}(buf_n, \langle m_n, r_n \rangle) = \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle) \cup \{buf_n\}$$

Let  $buf$  be an arbitrary prefix in  $\text{prefix}(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

1.  $buf \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . The proof is similar to the case FETCH-PREDICT-BRANCH-JMP.

2.  $buf \notin \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ , in which case  $buf = buf_n = buf_{n-1} \cdot inst @ \varepsilon \cdot pc \leftarrow (1 + 1:L) @ \varepsilon$ . Because  $\neg \text{transient}(c_{n-1})$  and because reorder buffers are well-formed (Lemma 2), we have from Definition 18 that  $buf_{n-1} \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have

$$\langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1} = \alpha_j \text{ where } j = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf_{n-1}|)$$

In the following, we let  $\alpha_j = \langle r_j, m_j \rangle$ . From Corollary 2 and  $(1:\_) = \llbracket pc \rrbracket_{\text{apl}(buf_{n-1}, r_{n-1})}$ , we have  $r_j(pc) = (1:\_)$  and hence  $lst\_pc(c_{n-1}) = 1$ , meaning that  $P[lst\_pc(c_{n-1})] \notin \{ \mathbf{beqz}_{\_}, \mathbf{jmp}_{\_} \}$ . From this, Definition 19, and  $|buf| = |buf_{n-1}| + 2$ , we get  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)(|buf|) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf_{n-1}|) + 1 = j + 1$ .

Additionally, from Definition 15, we have that  $\langle m_n, r_n \rangle \uplus buf = ((\langle m_n, r_n \rangle \uplus buf_{n-1}) \uplus inst @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon$ . From  $\langle m_{n-1}, r_{n-1} \rangle = \langle m_n, r_n \rangle$ , and the definition of  $\alpha_j$ , this gives us  $\langle m_n, r_n \rangle \uplus buf = (\tilde{\alpha}_j \uplus inst @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon$ . Hence, in order to show  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$  (which concludes our goal (G) for this case), it remains to show

$$(\tilde{\alpha}_j \uplus inst @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \alpha_{j+1}$$

The proof follows by case analysis on the instruction  $inst$ :

- (a)  $inst = x \leftarrow e$ . In this case, from Definition 15, we have  $(\tilde{\alpha}_j \uplus x \leftarrow e @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \langle m_j, r_j[x \mapsto \llbracket e \rrbracket_{r_j}][pc \mapsto 1 + 1] \rangle$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 8, rule ASSIGN), we also have  $\alpha_{j+1} = \langle m_j, r_j[x \mapsto \llbracket e \rrbracket_{r_j}][pc \mapsto 1 + 1] \rangle$ , which concludes  $(\tilde{\alpha}_j \uplus inst @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \alpha_{j+1}$ .
- (b)  $inst = x \leftarrow \mathbf{load} e$  and  $inst = \mathbf{store} e_a e_v$ . Similar to the previous case, these follow by Definition 15 and by inspection of the evaluation rules of the sequential semantics (Fig. 8, rule LOAD and STORE).
- (c) Other cases are not possible from  $inst \notin \{ \mathbf{beqz}_{\_}, \mathbf{jmp}_{\_} \}$  and because the program does not contain direct assignments to  $pc$  (cf. Lemma 1).

**Execute directive.** In this case, we have  $d = \text{execute } j$  and from Definition 19  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)$ . The proof proceeds by case analysis on the evaluation rule (Figs. 5 and 6). Notice that in all rules for the execute directive, we have  $m_n = m_{n-1}$  and  $r_n = r_{n-1}$ .

BRANCH-COMMIT: from the evaluation rules (cf. Fig. 5), we have:

$$buf_{n-1} = buf_{n-1}[1..j-1] \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufn-1})$$

$$buf_n = buf_{n-1}[1..j-1] \cdot pc \leftarrow (1:L) @ \varepsilon \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufi})$$

with  $P[1_0] = \mathbf{beqz} e 1'$ . Furthermore, we have  $1 = (\text{if } c = 0 \text{ then } 1' \text{ else } 1_0 + 1)$  where  $(c:\_) = \llbracket e \rrbracket_{\text{aplsan}(buf_{n-1}[0..j-1], r_{n-1})}$ , meaning that:

$$\text{goodpred}(buf_{n-1}[j], 1_0, \langle m_{n-1}, r_{n-1} \rangle) \quad (\text{Hpred})$$

Let  $buf$  be an arbitrary prefix in  $\text{prefix}(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . In this case, by Definition 18 and (Hbufn-1) and (Hbufi), and because  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , we also have that  $buf \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|)}$ . From  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$ .
- $|buf| \geq j$ . Notice that, by Definition 18 and  $buf \in \text{prefix}(buf_n, \langle m_n, r_n \rangle)$ , there is no mispredicted instruction in  $buf$  (except possibly the last one). Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf[j+1..|buf|]$  belongs to  $\text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf'|)}$ . From  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$ . Finally, from (Hpred), we have that  $\langle m_n, r_n \rangle \uplus buf' = \langle m_n, r_n \rangle \uplus buf$ , which concludes  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$ .

BRANCH-ROLLBACK from the evaluation rules (cf. Fig. 5), we have:

$$buf_{n-1} = buf_{n-1}[1..j-1] \cdot pc \leftarrow (1:\_) @ 1_0 \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufn-1})$$

$$buf_n = buf_{n-1}[1..j-1] \cdot pc \leftarrow (1'':L) @ \varepsilon \quad (\text{Hbufi})$$

with  $P[1_0] = \mathbf{beqz} e 1'$ .

Let  $buf$  be an arbitrary prefix in  $\text{prefix}(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the rule BRANCH-COMMIT.
- $|buf| = j$ . Notice that, by Definition 18 and  $buf \in prefix(buf_n, \langle m_n, r_n \rangle)$ , there is no mispredicted instruction in  $buf$  (except the last one). Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot pc \leftarrow (1:\_)@1_0$  belongs to  $prefix(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n-1)}(|buf'|)$ . From  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $corr_{\bar{a}, \bar{c}}(n) = corr_{\bar{a}, \bar{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ . Finally, from Definition 15, we have that  $\langle m_n, r_n \rangle \uplus buf' = \langle m_n, r_n \rangle \uplus buf$ , which concludes  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ .

JMP-COMMIT The proof for this case is similar to the proof for the case BRANCH-COMMIT.

JMP-ROLLBACK The proof for this case is similar to the proof for the case BRANCH-ROLLBACK.

EXECUTE-LOAD-PREDICT: from the evaluation rules (cf. Fig. 6), we have:

$$buf_{n-1} = buf_{n-1}[1..j-1] \cdot x \leftarrow \mathbf{load} e @ T \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufn-1})$$

$$buf_n = buf_{n-1}[1..j-1] \cdot x \leftarrow (v:L)@1_0 \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufi})$$

with  $(1_0:\_) = \llbracket pc \rrbracket_{aplsan}(buf_{n-1}[0..j-1], r_{n-1})$ . Notice that from Definition 16, we also have that  $P[1_0] = x \leftarrow \mathbf{load} e$ .

Let  $buf$  be an arbitrary prefix in  $prefix(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the rule BRANCH-COMMIT.
- $|buf| \geq j$ . Notice that, by Definition 18 and  $buf \in prefix(buf_n, \langle m_n, r_n \rangle)$ , there is no mispredicted instruction in  $buf$  (except possibly the last one). Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot x \leftarrow \mathbf{load} e @ T \cdot buf[j+1..|buf|]$  belongs to  $prefix(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n-1)}(|buf'|)$ . From  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $corr_{\bar{a}, \bar{c}}(n) = corr_{\bar{a}, \bar{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ . Finally, because  $P[1_0] = x \leftarrow \mathbf{load} e$ , we have that  $\langle m_n, r_n \rangle \uplus buf' = \langle m_n, r_n \rangle \uplus buf$ , which concludes  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ .

EXECUTE-LOAD-COMMIT: from the evaluation rules (cf. Fig. 6), we have:

$$buf_{n-1} = buf_{n-1}[1..j-1] \cdot x \leftarrow (m_{n-1}(a):s)@1_0 \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufn-1})$$

$$buf_n = buf_{n-1}[1..j-1] \cdot x \leftarrow (m_{n-1}(a):s_m(a))@e \cdot buf_{n-1}[j+1..|buf_{n-1}|] \quad (\text{Hbufi})$$

with  $P[1_0] = x \leftarrow \mathbf{load} e$ ,  $a = \llbracket e \rrbracket_{aplsan}(buf_{n-1}[1..j-1], r_{n-1})$ , and  $\mathbf{store} \_ \notin buf_{n-1}[1..j-1]$ .

Let  $buf$  be an arbitrary prefix in  $prefix(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the rule BRANCH-COMMIT.
- $|buf| \geq j$ . Notice that, by Definition 18 and  $buf \in prefix(buf_n, \langle m_n, r_n \rangle)$ , there is no mispredicted instruction in  $buf$  (except possibly the last one). Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot x \leftarrow (v:s)@1_0 \cdot buf[j+1..|buf|]$  belongs to  $prefix(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n-1)}(|buf'|)$ . From  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $corr_{\bar{a}, \bar{c}}(n) = corr_{\bar{a}, \bar{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ . Let  $\langle m', r' \rangle = \langle m_n, r_n \rangle \uplus buf_{n-1}[1..j-1]$ . Notice that from Lemma 4,  $r_n = r_{n-1}$  and  $a = \llbracket e \rrbracket_{aplsan}(buf_{n-1}[1..j-1], r_{n-1})$  we also have that  $\llbracket e \rrbracket_{r'}$ . Moreover, because  $\mathbf{store} \_ \notin buf_{n-1}[1..j-1]$  and  $m_n = m_{n-1}$ , we have  $m_{n-1} = m'$ , which implies  $m_{n-1}(a) = m'(a)$ . Hence, from this and Definition 15, we get that  $\langle m_n, r_n \rangle \uplus buf' = \langle m_n, r_n \rangle \uplus buf$  which concludes  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\bar{a}, \bar{c}}(n)}(|buf|)$ .

EXECUTE-LOAD-ROLLBACK from the evaluation rules (cf. Fig. 6), we have:

$$buf_{n-1} = buf_{n-1}[1..j-1] \cdot x \leftarrow (v:s)@1_0 \cdot pc \stackrel{*}{\leftarrow} (1:s)@e \cdot buf_{n-1}[j+2..|buf_{n-1}|]$$

$$buf_n = buf_{n-1}[1..j-1] \cdot x \leftarrow (m_{n-1}(a):s_m(a))@e \cdot pc \stackrel{*}{\leftarrow} (1:s)@e$$

with  $P[1_0] = x \leftarrow \mathbf{load} e$ ,  $a = \llbracket e \rrbracket_{aplsan}(buf_{n-1}[1..j-1], r_{n-1})$  and  $\mathbf{store} \_ \notin buf_{n-1}[1..j-1]$ .

Let  $buf$  be an arbitrary prefix in  $prefix(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the rule BRANCH-COMMIT.
- $|buf| \geq j$ . Notice that, by Definition 18, Lemma 2 and  $buf \in \text{prefix}(buf_n, \langle m_n, r_n \rangle)$ , we have  $buf = buf_n$  and there is no mispredicted instruction in  $buf$ . Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot x \leftarrow (v:s)@l_0 \cdot pc \xleftarrow{*} (1:s)@e$  belongs to  $\text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)}(|buf'|)$ . From  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)}(|buf|)$ .

From there, it suffices to show  $\langle m_n, r_n \rangle \uplus buf' = \langle m_n, r_n \rangle \uplus buf$  to get to our goal  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)}(|buf|)$ .

Let  $\langle m', r' \rangle = \langle m_n, r_n \rangle \uplus buf_{n-1}[1..j-1]$ . By Definition 15 and definitions of  $buf$  and  $buf'$ , we have:  $\langle m_n, r_n \rangle \uplus buf = \langle m', r' \rangle \uplus x \leftarrow (m_{n-1}(\mathbf{a}):s_m(\mathbf{a}))@e \cdot pc \xleftarrow{*} (1:s)@e$  and  $\langle m_n, r_n \rangle \uplus buf' = \langle m', r' \rangle \uplus x \leftarrow (v:s)@l_0 \cdot pc \xleftarrow{*} (1:s)@e$ .

Because  $\text{store}_{-} \notin buf_{n-1}[1..j-1]$  and  $m_n = m_{n-1}$ , we have  $m' = m_{n-1}$ . From this and Definition 15, we get  $\langle m_n, r_n \rangle \uplus buf = \langle m_{n-1}, r' [x \mapsto (m_{n-1}(\mathbf{a}):s_m(\mathbf{a}))] \rangle \uplus pc \xleftarrow{*} (1:s)@e$  and  $\langle m_n, r_n \rangle \uplus buf' = \langle m_{n-1}, r' [x \mapsto (m_{n-1}(\mathbf{a}):s_m(\mathbf{a}))] \rangle \uplus pc \xleftarrow{*} (1:s)@e$ . Hence, we simply have to show  $\llbracket e \rrbracket_{r'} = \mathbf{a}$ , which follows from Lemma 4, and definition of  $\mathbf{a}$ .

EXECUTE-ASSIGN: from the hardware evaluation rules (cf. Fig. 6), we have:

$$\begin{aligned} buf_{n-1} &= buf_{n-1}[1..j-1] \cdot r \leftarrow e@T \cdot buf_{n-1}[j+1..|buf_{n-1}|] \\ buf_n &= buf_{n-1}[1..j-1] \cdot r \leftarrow (v:s)@T \cdot buf_{n-1}[j+1..|buf_{n-1}|] \end{aligned}$$

with  $e \notin \hat{\mathcal{V}}$  and  $(v:s) = \llbracket e \rrbracket_{\text{apl}(buf_{n-1}[1..j-1], r_{n-1})}$ .

Let  $buf$  be an arbitrary prefix in  $\text{prefix}(buf_n, \langle m_n, r_n \rangle)$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the rule BRANCH-COMMIT.
- $|buf| \geq j$ . Notice that, by Definition 18 and  $buf \in \text{prefix}(buf_n, \langle m_n, r_n \rangle)$ , there is no mispredicted instruction in  $buf$  (except possibly the last one). Therefore, it follows from  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , that  $buf' = buf[1..j-1] \cdot r \leftarrow e@T \cdot buf[j+1..|buf|]$  belongs to  $\text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have that  $\langle m_{n-1}, r_{n-1} \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)}(|buf'|)$ . From this,  $|buf'| = |buf|$ ,  $\langle m_n, r_n \rangle = \langle m_{n-1}, r_{n-1} \rangle$ , and  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1)$ , we get that  $\langle m_n, r_n \rangle \uplus buf' = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)}(|buf|)$ . Let  $\langle m', r' \rangle = \langle m_n, r_n \rangle \uplus buf_{n-1}[1..j-1]$ . Notice that from Lemma 4,  $r_n = r_{n-1}$  and  $(v:s) = \llbracket e \rrbracket_{\text{apl}(buf_{n-1}[1..j-1], r_{n-1})}$ , we get  $(v:s) = \llbracket e \rrbracket_{r'}$ . Moreover, because  $buf_{n-1}$  is well formed (cf. Lemma 2), from Definition 16 and  $e \in \hat{\mathcal{V}}$ , we know that  $T = \varepsilon$ . Therefore, by Definition 15 and rewriting we get

$$\begin{aligned} \langle m_n, r_n \rangle \uplus buf' &= \langle m', r' \rangle \uplus r \leftarrow e@T \cdot buf[j+1..|buf|] \\ &= \langle m', r' \rangle \uplus r \leftarrow (v:s)@e \cdot buf[j+1..|buf|] \\ &= \langle m_n, r_n \rangle \uplus buf \end{aligned}$$

which by  $\langle m_n, r_n \rangle \uplus buf = \alpha_{\text{corr}_{\tilde{\alpha}, \tilde{c}}(n)}(|buf|)$  concludes (G).

EXECUTE-STORE: The proof is similar to the case EXECUTE-ASSIGN.

**Retire directive.** In this case, from Definition 19, we have  $\text{corr}_{\tilde{\alpha}, \tilde{c}}(n) = \text{shift}(\text{corr}_{\tilde{\alpha}, \tilde{c}}(n-1))$ . The proof proceeds by case analysis on the evaluation rule.

RETIRE-ASSIGN: In this case, from the hardware evaluation rules in Fig. 7, we have  $buf_{n-1} = r \leftarrow (v:s)@e \cdot buf_n$ ,  $m_n = m_{n-1}$  and  $r_n = r_{n-1}[r \mapsto (v:s)]$ . We consider two cases:

- $r \neq pc$ . In this case, because  $buf_{n-1}$  is well-formed (cf. Lemma 2) and from the definition of well-formed buffers (Definition 16), we have that  $buf_n = pc \xleftarrow{*} (1:L) \cdot buf'_{n-1}$ . Hence, from Definition 18, we have

$$\begin{aligned} \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle) &= \{\varepsilon\} \cup \{r \leftarrow (v:s)@e \cdot pc \leftarrow (1:L)@e \cdot buf'_{n-1} \mid \\ &\quad buf'_{n-1} \in \text{prefix}(buf'_{n-1}, \langle m_{n-1}, r_{n-1} \rangle) \uplus r \leftarrow (v:s)@e \cdot pc \leftarrow (1:L)@e\} \\ \text{prefix}(buf_n, \langle m_n, r_n \rangle) &= \{\varepsilon\} \cup \{pc \leftarrow (1:L)@e \cdot buf'_{n-1} \mid buf'_{n-1} \in \text{prefix}(buf'_{n-1}, \langle m_n, r_n \rangle) \uplus pc \leftarrow (1:L)@e\} \end{aligned}$$



Let  $buf$  be an arbitrary prefix in  $buf_n$ . By Definition 18 and the definition of  $buf_n$  and  $buf_{n-1}$ , we have that  $r \leftarrow (v:s)@ \varepsilon \cdot buf$  is a prefix in  $prefix(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$ . Hence, from (IH), we have  $\langle m_{n-1}, r_{n-1} \rangle \uplus r \leftarrow (v:s)@ \varepsilon \cdot buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . Hence, by Definition 15, we get  $\langle m_{n-1}, r_{n-1} [r \mapsto (v:s)] \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . By  $m_n = m_{n-1}$  and  $r_n = r_{n-1} [r \mapsto (v:s)]$ , this gives us  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . Finally, by the definition of *shift*, we get  $\langle m_n, r_n \rangle \uplus buf = \alpha_{shift(corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|))}$ , which from  $corr_{\tilde{\alpha}, \tilde{c}}(n) = shift(corr_{\tilde{\alpha}, \tilde{c}}(n-1))$ , entails  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$  and concludes (G).

- $r = pc$ . In this case, from Definition 18, we have

$$prefix(buf_{n-1}) = \{\varepsilon\} \cup \{pc \leftarrow (v:s)@ \varepsilon \cdot buf' \mid buf' \in prefix(buf_n, \langle m, r \rangle \uplus pc \leftarrow (v:s)@ \varepsilon)\}$$

Let  $buf$  be an arbitrary prefix in  $buf_n$ . By Definition 18 and the definition of  $buf_{n-1}$ , we have that  $pc \leftarrow (v:s)@ \varepsilon \cdot buf$  is a prefix in  $prefix(buf_{n-1})$ . Hence, from (IH), we have  $\langle m_{n-1}, r_{n-1} \rangle \uplus pc \leftarrow (v:s)@ \varepsilon \cdot buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . Hence, by Definition 15, we get  $\langle m_{n-1}, r_{n-1} [pc \mapsto (v:s)] \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . By  $m_n = m_{n-1}$  and  $r_n = r_{n-1} [pc \mapsto (v:s)]$ , this gives us  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|+1)}$ . Finally, by the definition of *shift*, we get  $\langle m_n, r_n \rangle \uplus buf = \alpha_{shift(corr_{\tilde{\alpha}, \tilde{c}}(n-1)(|buf|))}$ , which from  $corr_{\tilde{\alpha}, \tilde{c}}(n) = shift(corr_{\tilde{\alpha}, \tilde{c}}(n-1))$ , entails  $\langle m_n, r_n \rangle \uplus buf = \alpha_{corr_{\tilde{\alpha}, \tilde{c}}(n)(|buf|)}$  and concludes (G).

RETIRE-ASSIGN-MARKED: The proof for this case is similar to the proof for the rule RETIRE-ASSIGN, case  $r = pc$ .

RETIRE-STORE-LOW and RETIRE-STORE-HIGH The proof for this case is similar to the proof for the rule RETIRE-ASSIGN.

We have shown for any evaluation rule in the hardware semantics that if (G) holds at step  $n-1$ , then it also holds at step  $i$ . This concludes the proof of Lemma 5.  $\square$

## E.2 Low-equivalence relations between pairs of executions

For the proofs, we refine the low-projection in order to distinguish secret values in  $\hat{\mathcal{V}}$  from undefined values ( $\perp$ )<sup>10</sup>. This refined low-projection discloses public values and undefined values ( $\perp$ ), and replaces secret with a special symbol  $\blacksquare$ .

**Definition 20** (Refined low-projection).

$$\|(v:L)\|_L = (v:L) \qquad \|(v:H)\|_L = \blacksquare \qquad \|\perp\|_L = \perp$$

We let  $r|_L$  be the point-wise extension of  $\cdot|_L$  to register maps.

Similarly, we define a refined low buffer projection that replaces secrets with  $\blacksquare$  instead of  $\perp$ :

**Definition 21** (Refined low buffer projection  $\|buf\|_L$ ). For all reorder buffer  $buf$  its refined low-projection  $\|buf\|_L$  is given by:

$$\begin{aligned} \|e\|_L &= \begin{cases} \blacksquare & \text{if } e = (v:H) \\ e & \text{otherwise} \end{cases} \\ \|\varepsilon\|_L &= \varepsilon \\ \|r \leftarrow e\|_L &= r \leftarrow \|e\|_L \\ \|x \leftarrow \mathbf{load } e\|_L &= x \leftarrow \mathbf{load } \|e\|_L \\ \|\mathbf{store } e_a e_v\|_L &= \mathbf{store } \|e_a\|_L \|e_v\|_L \\ \|\mathbf{inst } @T \cdot buf\|_L &= \|\mathbf{inst}\|_L @T \cdot \|buf\|_L \end{aligned}$$

The following lemma expresses that low-projections and refined low-projection for values in  $\hat{\mathcal{V}}$  are equivalent.

**Lemma 6.** For all pairs of labeled values  $(v:s)$  and  $(v':s')$ ,

$$(v:s)|_L = (v':s')|_L \iff \|(v:s)\|_L = \|(v':s')\|_L$$

*Proof.* The proof directly follows from Definition 3 and Definition 20.  $\square$

**Corollary 4.** For all register maps  $r$  and  $r'$  such that  $r|_L = r'|_L$  and that do not contain unresolved values (i.e., for all register  $x$ ,  $r(x) \in \hat{\mathcal{V}}$ ), we have that  $\|r\|_L = \|r'\|_L$ .

<sup>10</sup>In particular, this is important to prove Lemma 14 and guarantee that two low-equivalent configuration can make progress at the same time

The following lemma expresses that equality of refined low-projections implies and equality of low-projections.

**Lemma 7.** For all pairs of (possibly undefined) value  $u, u' \in \hat{\mathcal{V}} \cup \{\perp\}$ ,

$$\|u\|_{\mathbb{L}} = \|u'\|_{\mathbb{L}} \implies u|_{\mathbb{L}} = u'|_{\mathbb{L}}$$

*Proof.* The proof goes by case analysis on  $u$ :

- Case  $u = (v:L)$ : from Definition 20 we have  $\|u\|_{\mathbb{L}} = \|u'\|_{\mathbb{L}} = (v:L)$ , meaning that  $u = u' = (v:L)$ . Therefore from Definition 3 we have  $u|_{\mathbb{L}} = u'|_{\mathbb{L}} = (v:L)$ ;
- Case  $u = (v:H)$ : from Definition 20 we have  $\|u\|_{\mathbb{L}} = \|u'\|_{\mathbb{L}} = \blacksquare$ , meaning that  $u = (v:H)$  and  $u' = (v:H)$ . Therefore from Definition 3 we have  $u|_{\mathbb{L}} = u'|_{\mathbb{L}} = \perp$ ;
- Case  $u = \perp$ : from Definition 20 we have  $\|u\|_{\mathbb{L}} = \|u'\|_{\mathbb{L}} = \perp$ , meaning that  $u = u' = \perp$ . Therefore from Definition 3 we have  $u|_{\mathbb{L}} = u'|_{\mathbb{L}} = \perp$ ;

□

**Corollary 5.** For all register maps  $r$  and  $r'$ :

$$\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}} \implies r|_{\mathbb{L}} = r'|_{\mathbb{L}}$$

*Proof.* The proof directly follows from Definition 20, Definition 3, and Lemma 7. □

The following lemma expresses that for two reorder buffer, if their refined low-projections are equal, then their low-projections are equal:

**Lemma 8.** For all reorder buffers  $buf$  and  $buf'$ :

$$\|buf\|_{\mathbb{L}} = \|buf'\|_{\mathbb{L}} \implies [buf]_{\mathbb{L}} = [buf']_{\mathbb{L}}$$

*Proof.* Notice that from  $\|buf\|_{\mathbb{L}} = \|buf'\|_{\mathbb{L}}$  and Definition 21,  $buf$  and  $buf'$  have the same size. The proof goes by induction on the size of  $buf$ .

**Base case** ( $buf = buf' = \epsilon$ ) is trivial.

**Inductive case.** Consider that Lemma 8 holds for reorder buffers of size  $n - 1$ ,  $buf_{n-1}$  and  $buf'_{n-1}$ . We show that Lemma 8 still holds for buffers of size  $n$ :

$$\|inst@T \cdot buf_{n-1}\|_{\mathbb{L}} = \|inst'@T' \cdot buf'_{n-1}\|_{\mathbb{L}} \implies \tag{2}$$

$$[inst@T \cdot buf_{n-1}]_{\mathbb{L}} = [inst'@T' \cdot buf'_{n-1}]_{\mathbb{L}} \tag{3}$$

By the induction hypothesis, Definition 21 and Definition 9, we this amounts to show that

$$\|inst@T\|_{\mathbb{L}} = \|inst'@T'\|_{\mathbb{L}} \implies [inst@T]_{\mathbb{L}} = [inst'@T']_{\mathbb{L}}$$

The proof continues by case analysis on  $inst$ . Because  $\|inst@T\|_{\mathbb{L}}$  is strictly equivalent to  $[inst@T]_{\mathbb{L}}$  except for expressions, it is sufficient to show that for any expressions  $e, e'$ ,

$$\|e\|_{\mathbb{L}} = \|e'\|_{\mathbb{L}} \implies [e]_{\mathbb{L}} = [e']_{\mathbb{L}}$$

The proof proceeds by case analysis of  $e$ :

- Case  $e = (v:H)$ : from Definition 21, we have that  $\|e\|_{\mathbb{L}} = \blacksquare$ . From the hypothesis  $\|e\|_{\mathbb{L}} = \|e'\|_{\mathbb{L}}$ , we also have  $\|e'\|_{\mathbb{L}} = \blacksquare$ , meaning that  $e' = (v':H)$ . Finally, from Definition 9, we have  $[e]_{\mathbb{L}} = [e']_{\mathbb{L}} = \perp$  which concludes our goal.
- Otherwise, from Definition 21, we have that  $\|e\|_{\mathbb{L}} = e$ . From the hypothesis  $\|e\|_{\mathbb{L}} = \|e'\|_{\mathbb{L}}$ , we also have  $\|e'\|_{\mathbb{L}} = e$ , meaning that  $e' = e$ . Finally, from Definition 9, we have  $[e]_{\mathbb{L}} = [e']_{\mathbb{L}} = e$  which concludes our goal.

□

The following lemma expresses that for values, the refined low-buffer projection and the refined low-equivalence relation are equivalent.

**Lemma 9.** For all values  $(v:s), (v':s') \in \hat{\mathcal{V}}$ :

$$\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L \iff \llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$$

*Proof.* We consider both sides of the equivalence separately:

$\implies$  We consider the two cases  $s = H$  and  $s = L$ :

- In case  $s = H$ , from Definition 21, we have  $\llbracket (v:s) \rrbracket_L = \blacksquare$ . Therefore, from  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ , we have  $\llbracket (v':s') \rrbracket_L = \blacksquare$ , meaning that  $s' = H$ . Finally,  $\llbracket (v:H) \rrbracket_L = \blacksquare$  and  $\llbracket (v':H) \rrbracket_L = \blacksquare$ , therefore  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ .
- In case  $s = L$ , from Definition 21, we have  $\llbracket (v:s) \rrbracket_L = (v:s)$ . Therefore, from  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ , we have  $\llbracket (v':s') \rrbracket_L = (v:s)$ , meaning that  $(v':s') = (v:s)$ , which entails  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ .

$\impliedby$  We consider the two cases  $s = H$  and  $s = L$ :

- In case  $s = H$ , by Definition 20, we have  $\llbracket (v:H) \rrbracket_L = \blacksquare$ . Therefore, from  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ , we have  $\llbracket (v':s') \rrbracket_L = \blacksquare$ , meaning that  $s' = H$ . Finally, by Definition 21, we have  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L = \blacksquare$ .
- In case  $s = L$ , by Definition 20, we have  $\llbracket (v:L) \rrbracket_L = (v:L)$ . Therefore, from  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ , we have  $\llbracket (v':s') \rrbracket_L = (v:L)$ , meaning that  $v = v'$  and  $s = s'$ , which entails  $\llbracket (v:s) \rrbracket_L = \llbracket (v':s') \rrbracket_L$ .

□

The following lemma expresses that speculations are disclosed in the refined low-projections of reorder buffers, meaning that two low-equivalent reorder buffers  $buf$  and  $buf'$  correspond both to sequential executions or both to speculative execution.

**Lemma 10.** For all reorder buffers  $buf$  and  $buf'$  such that  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$ :

$$\exists inst@T \in buf. T \neq \varepsilon \iff \exists inst'@T' \in buf'. T' \neq \varepsilon$$

*Proof.* Notice that from Definition 21,  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$ , implies the pointwise equality of  $\llbracket buf \rrbracket_L$  and  $\llbracket buf' \rrbracket_L$ . Therefore for each  $i^{th}$  instructions  $inst@T$  in  $buf$ , the corresponding  $i^{th}$  instructions  $inst'@T'$  in  $buf'$  satisfies  $\llbracket inst@T \rrbracket_L = \llbracket inst'@T' \rrbracket_L$ . Moreover, from Definition 21, we have that  $T = T'$ . Therefore,  $T \neq \varepsilon \iff T' \neq \varepsilon$ . □

The following proposition expresses that a register that is public in a reorder buffer  $buf$  and a register map  $r$ , is also public in  $apl(buf, r)$ .

**Lemma 11** (*apl* preserves security level). For all register  $r$ , register map  $r$  and reorder buffer  $buf$ :

$$\begin{aligned} (r(r) = (\_ : L) \vee r(r) = \perp) \wedge & \quad \text{(Hreg)} \\ (r \leftarrow (\_ : s)@T \in buf_n \implies s = L) & \quad \text{(Hbuf)} \\ \implies apl(buf, r)(r) = (\_ : L) \vee apl(buf, r)(r) = \perp & \end{aligned}$$

*Proof.* The proof that  $apl(buf, r)(r) = (\_ : L) \vee apl(buf, r)(r) = \perp$  goes by induction on the size of  $buf$ :

**Base case:**  $buf = \varepsilon$ . Consider a register map  $r$  such that (Hreg) hold. By Definition 2,  $apl(\varepsilon, r) = r$ . Hence,  $apl(\varepsilon, r)(r) = (\_ : L) \vee apl(\varepsilon, r)(r) = \perp$  directly follows from (Hreg).

**Inductive case.** Consider that Lemma 11 holds for a reorder buffer  $buf_{n-1}$  of size  $n-1$ . We show that it still holds for  $buf_n = inst@T \cdot buf_{n-1}$ . That is for a register map  $r$  such that (Hreg) hold and  $buf_n$  such that (Hbuf) hold, then  $apl(buf_n, r)(r) = (\_ : L) \vee apl(buf_n, r)(r) = \perp$ . The proof continues by case analysis on  $inst$ :

- Case  $inst = r \leftarrow (v:s)$ . From (Hbuf), we have that  $s = L$ . From Definition 2, we have that  $apl(inst@T \cdot buf_n, r) = apl(buf_{n-1}, r[r \mapsto (v:L)])$ . Because  $r[r \mapsto (v:L)]$  satisfies (Hreg), we can apply the induction hypothesis, which gives us  $apl(buf_{n-1}, r[r \mapsto (v:L)])(r)$  equals  $(\_ : L)$  or  $\perp$ , hence  $apl(buf_n, r)(r)$  equals  $(\_ : L)$  or  $\perp$ .

- Case  $inst = r' \leftarrow (v:s)$  with  $r \neq r'$ . From Definition 2, we have that  $apl(inst@T \cdot buf_n, r) = apl(buf_{n-1}, r[r' \mapsto (v:s)])$ . Because  $r[r' \mapsto (v:s)]$  satisfies (Hreg), we can apply the induction hypothesis, which gives us  $apl(buf_{n-1}, r[r' \mapsto (v:L)])(r)$  equals  $(\_ :L)$  or  $\perp$ , hence  $apl(buf_n, r)(r)$  equals  $(\_ :L)$  or  $\perp$ .
- Case  $inst = r' \leftarrow e$  where  $e \notin \hat{\mathcal{V}}$ . From Definition 2, we have that  $apl(inst@T \cdot buf_{n-1}, r) = apl(buf_{n-1}, r[r' \mapsto \perp])$ . Because  $r[r' \mapsto \perp]$  satisfies (Hreg), we can apply the induction hypothesis, which gives us  $apl(buf_{n-1}, r[r' \mapsto (v:L)])(r)$  equals  $(\_ :L)$  or  $\perp$ , hence  $apl(buf_n, r)(r)$  equals  $(\_ :L)$  or  $\perp$ .
- Case  $inst = r' \leftarrow \mathbf{load} \_ :$  the proof is similar to the previous case.
- Case  $inst = \mathbf{store} \_ :$  from Definition 2, we have that  $apl(inst@T \cdot buf_{n-1}, r) = apl(buf_{n-1}, r)$ . Hence,  $apl(buf_n, r)(r) = (\_ :L) \vee apl(buf_n, r)(r) = \perp$  directly follows from the induction hypothesis.  $\square$

The following lemma expresses that the function  $apl$  applied to two low-equivalent buffers and two low-equivalent register maps returns two low equivalent register maps:

**Lemma 12.** *For all register maps  $r$  and  $r'$  and buffers  $buf$  and  $buf'$ :*

$$\|r\|_L = \|r'\|_L \wedge \|buf\|_L = \|buf'\|_L \implies \|apl(buf, r)\|_L = \|apl(buf', r')\|_L$$

*Proof.* First, notice that from the hypothesis  $\|buf\|_L = \|buf'\|_L$  and Definition 21, we have,  $|buf| = |buf'|$ . The proof goes by induction on the size of  $buf$  and  $buf'$ .

**Base case:**  $buf = buf' = \varepsilon$ . By Definition 2,  $apl(\varepsilon, r) = r$  and  $apl(\varepsilon, r') = r'$ . Hence,  $\|apl(buf, r)\|_L = \|apl(buf', r')\|_L$  directly follows from the hypothesis  $\|r\|_L = \|r'\|_L$ .

**Inductive case.** Consider that Lemma 12 holds for reorder buffers of size  $n-1$ ,  $buf_{n-1}$  and  $buf'_{n-1}$ , meaning that for all register maps  $r, r'$ :

$$\|r\|_L = \|r'\|_L \wedge \|buf_{n-1}\|_L = \|buf'_{n-1}\|_L \implies \|apl(buf_{n-1}, r)\|_L = \|apl(buf'_{n-1}, r')\|_L \quad (\text{IH})$$

We show that Lemma 12 still holds for buffers of size  $n$ , meaning that for all register maps  $r, r'$ :

$$\begin{aligned} \|r\|_L &= \|r'\|_L \wedge & (\text{Hreg}) \\ \|inst@T \cdot buf_{n-1}\|_L &= \|inst'@T \cdot buf'_{n-1}\|_L \implies & (\text{Hbufn}) \\ \|apl(inst@T \cdot buf_{n-1}, r)\|_L &= \|apl(inst'@T \cdot buf'_{n-1}, r')\|_L & (\text{G}) \end{aligned}$$

From (Hbufn) and Definition 21, we have:

$$\|inst\|_L = \|inst'\|_L \quad (\text{Hinst})$$

and

$$\|buf_{n-1}\|_L = \|buf'_{n-1}\|_L \quad (\text{Hbufn-1})$$

The proof continues by case analysis on  $inst$ :

- Case  $inst = \mathbf{store} \_ :$  from Definition 21, we have that  $\|inst\|_L = \mathbf{store} \_ :$ . From (Hinst), we also have  $\|inst'\|_L = \mathbf{store} \_ :$ , meaning that  $inst' = \mathbf{store} \_ :$ . From Definition 2, we have:

$$\begin{aligned} apl(inst@T \cdot buf_{n-1}, r) &= apl(buf_{n-1}, r) \text{ and} \\ apl(inst'@T \cdot buf'_{n-1}, r) &= apl(buf'_{n-1}, r') \end{aligned}$$

Therefore, (G) follows from the application of (IH) with (Hreg) and (Hbufn-1).

- Case  $inst = x \leftarrow \mathbf{load} \_ :$  from Definition 21, we have that  $\|inst\|_L = x \leftarrow \mathbf{load} \_ :$ . From (Hinst), we also have  $\|inst'\|_L = x \leftarrow \mathbf{load} \_ :$ , meaning that  $inst' = x \leftarrow \mathbf{load} \_ :$ . From Definition 2, we have:

$$\begin{aligned} apl(inst@T \cdot buf_{n-1}, r) &= apl(buf_{n-1}, r[x \mapsto \perp]) \text{ and} \\ apl(inst'@T \cdot buf'_{n-1}, r) &= apl(buf'_{n-1}, r'[x \mapsto \perp]) \end{aligned}$$

Finally, from Definition 20 and (Hreg), we have  $\|r[x \mapsto \perp]\|_L = \|r'[x \mapsto \perp]\|_L$ . Therefore, (G) follows from the application of (IH) with (Hbufn-1) and  $\|r[x \mapsto \perp]\|_L = \|r'[x \mapsto \perp]\|_L$ .



- Case  $inst = r \leftarrow e$  where  $e \notin \hat{\mathcal{V}}$ : from Definition 21,  $\llbracket inst \rrbracket_L = r \leftarrow e$ . From (Hinst), we also have  $\llbracket inst' \rrbracket_L = r \leftarrow e$ , meaning that  $inst' = r \leftarrow e$ . From Definition 2, we have:

$$\begin{aligned} apl(inst @ T \cdot buf_{n-1}, r) &= apl(buf_{n-1}, r[x \mapsto \perp]) \text{ and} \\ apl(inst' @ T \cdot buf'_{n-1}, r) &= apl(buf'_{n-1}, r'[x \mapsto \perp]) \end{aligned}$$

The rest of the proof is similar to case  $inst = x \leftarrow \mathbf{load} \_$ .

- Case  $inst = r \leftarrow (v:L)$ : from Definition 21,  $\llbracket inst \rrbracket_L = (v:L)$ . From (Hinst), we also have  $\llbracket inst' \rrbracket_L = r \leftarrow (v:L)$ , meaning that  $inst' = r \leftarrow (v:L)$ . From Definition 2, we have:

$$\begin{aligned} apl(inst @ T \cdot buf_{n-1}, r) &= apl(buf_{n-1}, r[r \mapsto (v:L)]) \text{ and} \\ apl(inst' @ T \cdot buf'_{n-1}, r) &= apl(buf'_{n-1}, r'[r \mapsto (v:L)]) \end{aligned}$$

Finally, from Definition 20 and (Hreg), we have  $\|r[r \mapsto (v:L)]\|_L = \|r'[r \mapsto (v:L)]\|_L$ . Therefore, (G) follows from the application of (IH) with (Hbufn-1) and  $\|r[r \mapsto (v:L)]\|_L = \|r'[r \mapsto (v:L)]\|_L$ .

- Case  $inst = r \leftarrow (v:H)$ : from Definition 21,  $\llbracket inst \rrbracket_L = r \leftarrow \blacksquare$ . From (Hinst), we also have  $\llbracket inst' \rrbracket_L = r \leftarrow \blacksquare$ , meaning that  $inst' = r \leftarrow (v':H)$ . From Definition 2, we have:

$$\begin{aligned} apl(inst @ T \cdot buf_{n-1}, r) &= apl(buf_{n-1}, r[r \mapsto (v:H)]) \text{ and} \\ apl(inst' @ T \cdot buf'_{n-1}, r) &= apl(buf'_{n-1}, r'[r \mapsto (v':H)]) \end{aligned}$$

Finally, from Definition 20 and (Hreg), we have  $\|r[r \mapsto (v:H)]\|_L = \|r'[r \mapsto (v':H)]\|_L$ . Therefore, (G) follows from the application of (IH) with (Hbufn-1) and  $\|r[r \mapsto (v:H)]\|_L = \|r'[r \mapsto (v':H)]\|_L$ . □

The following lemma expresses that the function *aplsan* applied to two low-equivalent buffers and two low-equivalent register maps returns two low equivalent register maps.

**Lemma 13.**  $\|r\|_L = \|r'\|_L \wedge \llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L \implies \|\mathit{aplsan}(buf, r)\|_L = \|\mathit{aplsan}(buf', r')\|_L$

*Proof.* We consider the two cases in Definition 5:

- **Sequential execution** ( $\forall inst @ T \in buf. T = \varepsilon$ ): In this case,  $\mathit{aplsan}(buf, r) = apl(buf, r)$ . From the hypothesis  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$  and Lemma 10, we also have  $\forall inst @ T \in buf'. T = \varepsilon$ . Therefore,  $\mathit{aplsan}(buf', r') = apl(buf', r')$ . Consequently, to show  $\|\mathit{aplsan}(buf, r)\|_L = \|\mathit{aplsan}(buf', r')\|_L$ , we have to show  $\|apl(buf, r)\|_L = \|apl(buf', r')\|_L$ . This follows from the application of Lemma 12 with  $\|r\|_L = \|r'\|_L$  and  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$ .
- **Speculative execution** ( $\exists inst @ T \in buf. T \neq \varepsilon$ ): In this case,  $\mathit{aplsan}(buf, r) = apl(buf, r)|_L$ . From the hypothesis  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$  and Lemma 10, we also have  $\exists inst @ T \in buf'. T \neq \varepsilon$ . Therefore,  $\mathit{aplsan}(buf', r') = apl(buf', r')|_L$ . Consequently, to show  $\|\mathit{aplsan}(buf, r)\|_L = \|\mathit{aplsan}(buf', r')\|_L$ , we have to show  $\|apl(buf, r)|_L\|_L = \|apl(buf', r')|_L\|_L$ , which amounts to show  $apl(buf, r)|_L = apl(buf', r')|_L$ . By Lemma 7, we have that  $apl(buf, r)|_L = apl(buf', r')|_L$  follows from  $\|apl(buf, r)\|_L = \|apl(buf', r')\|_L$ , which in turns follows from the application of Lemma 12 with  $\|r\|_L = \|r'\|_L$  and  $\llbracket buf \rrbracket_L = \llbracket buf' \rrbracket_L$ . □

The following lemma expresses that refined low projection can distinguish values from non values.

**Lemma 14.** For all (possibly unresolved) values  $u, u' \in \hat{\mathcal{V}} \cup \{\perp\}$  such that  $\|u\|_L = \|u'\|_L$ .  $u \in \hat{\mathcal{V}} \iff u' \in \hat{\mathcal{V}}$

*Proof.* The proof goes by case analysis on  $u$ :

- Case  $u = (v:L)$ : we have  $\|u\|_L = \|u'\|_L = (v:L)$ , therefore  $u' = (v:L)$ , meaning that  $u, u' \in \hat{\mathcal{V}}$ ;
- Case  $u = (v:H)$ : we have  $\|u\|_L = \|u'\|_L = \blacksquare$ , therefore  $u' = (v':H)$ , meaning that  $u, u' \in \hat{\mathcal{V}}$ ;

- Case  $u = \perp$ : we have  $\|u\|_{\mathbb{L}} = \|u'\|_{\mathbb{L}} = \perp$ , therefore  $u' = \perp$ , meaning that  $u, u' \notin \hat{\mathcal{V}}$ .

□

**Corollary 6.** For all register maps  $r$  and  $r'$  such that  $\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}}$  and for all register  $x$ .  $r(x) \in \hat{\mathcal{V}} \iff r'(x) \in \hat{\mathcal{V}}$

*Proof.* This directly follows from Lemma 14 and the definition of the refined low-projection for register maps (Definition 20). □

The following lemma expresses that the evaluation of an expression with two low-equivalent register maps returns low-equivalent values.

**Lemma 15.** For all register maps  $r$  and  $r'$  such that  $\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}}$  and for all expression  $e$ , either both  $\llbracket e \rrbracket_r$  and  $\llbracket e \rrbracket_{r'}$  are undefined, or  $\|\llbracket e \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e \rrbracket_{r'}\|_{\mathbb{L}}$ .

*Proof.* The proof goes by induction on the expression evaluation rules (cf. Fig. 3).

**Base cases:**

- Case  $e = (v:s)$ :  $\llbracket (v:s) \rrbracket_r$  and  $\llbracket (v:s) \rrbracket_{r'}$  both evaluate to  $(v:s)$ , therefore  $\|\llbracket (v:s) \rrbracket_r\|_{\mathbb{L}} = \|\llbracket (v:s) \rrbracket_{r'}\|_{\mathbb{L}}$ ;
- Case  $e = x$  and  $r(x) \in \hat{\mathcal{V}}$ : From the hypothesis  $\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}}$  and Corollary 6, we have  $r'(x) \in \hat{\mathcal{V}}$ . Therefore,  $\llbracket x \rrbracket_r = r(x)$  and  $\llbracket x \rrbracket_{r'} = r'(x)$ . From the hypothesis  $\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}}$  and Definition 20, we have  $\|r(x)\|_{\mathbb{L}} = \|r'(x)\|_{\mathbb{L}}$ , which entails  $\|\llbracket x \rrbracket_r\|_{\mathbb{L}} = \|\llbracket x \rrbracket_{r'}\|_{\mathbb{L}}$ ;
- Case  $e = x$  and  $r(x) \notin \hat{\mathcal{V}}$ : From the hypothesis  $\|r\|_{\mathbb{L}} = \|r'\|_{\mathbb{L}}$  and Corollary 6, we have  $r'(x) \notin \hat{\mathcal{V}}$ . Therefore, both  $\llbracket x \rrbracket_r$  and  $\llbracket x \rrbracket_{r'}$  are undefined.

**Inductive case:** Case  $e = e_1 \otimes e_2$ . Consider two expressions  $e_1$  and  $e_2$  such that Lemma 15 holds, meaning that:

$$\begin{aligned} &\text{Either both } \llbracket e_1 \rrbracket_r \text{ and } \llbracket e_1 \rrbracket_{r'} \text{ are undefined or } \|\llbracket e_1 \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e_1 \rrbracket_{r'}\|_{\mathbb{L}} \text{ and} \\ &\text{either both } \llbracket e_2 \rrbracket_r \text{ and } \llbracket e_2 \rrbracket_{r'} \text{ are undefined or } \|\llbracket e_2 \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e_2 \rrbracket_{r'}\|_{\mathbb{L}} \end{aligned} \quad (\text{IH})$$

To show  $\|\llbracket e_1 \otimes e_2 \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e_1 \otimes e_2 \rrbracket_{r'}\|_{\mathbb{L}}$ , we have to consider the following cases:

- Case  $\llbracket e_1 \rrbracket_r$  or  $\llbracket e_2 \rrbracket_r$  is undefined. In this case, from (IH) we also have  $\llbracket e_1 \rrbracket_{r'}$  or  $\llbracket e_2 \rrbracket_{r'}$  is undefined. Therefore, both  $\llbracket e_1 \otimes e_2 \rrbracket_r$  and  $\llbracket e_1 \otimes e_2 \rrbracket_{r'}$  are undefined.
- Case  $\llbracket e_1 \rrbracket_r = (v_1:L)$  and  $\llbracket e_2 \rrbracket_r = (v_2:L)$ . In this case, from (IH) and Definition 20, we also have  $\llbracket e_1 \rrbracket_{r'} = (v_1:L)$  and  $\llbracket e_2 \rrbracket_{r'} = (v_2:L)$ . Therefore, both  $\llbracket e_1 \otimes e_2 \rrbracket_r$  and  $\llbracket e_1 \otimes e_2 \rrbracket_{r'}$  evaluate to  $(v_1 \otimes v_2:L)$ , which entails  $\|\llbracket e_1 \otimes e_2 \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e_1 \otimes e_2 \rrbracket_{r'}\|_{\mathbb{L}}$ .
- Case  $\llbracket e_1 \rrbracket_r = (v_1:s_1)$  and  $\llbracket e_2 \rrbracket_r = (v_2:s_2)$  such that  $s_1 = H$  or  $s_2 = H$ . In this case, from (IH) and Definition 20, we also have  $\llbracket e_1 \rrbracket_{r'} = (v'_1:s'_1)$  and  $\llbracket e_2 \rrbracket_{r'} = (v'_2:s'_2)$  such that  $s'_1 = H$  or  $s'_2 = H$ . Consequently,  $\llbracket e_1 \otimes e_2 \rrbracket_r = (v_1 \otimes v_2:s_1 \sqcup s_2)$  with  $s_1 \sqcup s_2 = H$  and  $\llbracket e_1 \otimes e_2 \rrbracket_{r'} = (v'_1 \otimes v'_2:s'_1 \sqcup s'_2)$  with  $s'_1 \sqcup s'_2 = H$ . Finally, because  $\|(v_1 \otimes v_2:H)\|_{\mathbb{L}} = \|(v'_1 \otimes v'_2:H)\|_{\mathbb{L}} = \blacksquare$ , we have  $\|\llbracket e_1 \otimes e_2 \rrbracket_r\|_{\mathbb{L}} = \|\llbracket e_1 \otimes e_2 \rrbracket_{r'}\|_{\mathbb{L}}$ .

□

### E.3 Proof of security for constant-time programs without declassification

The following hypotheses are used to prove security for constant-time programs without declassification:

**Hypothesis 1.** The functions *predict*, *update*, and *next* are deterministic.

**Hypothesis 2.** The program is constant-time and does not declassify secret data (according to Definition 6). In particular, it means that for all configurations  $\langle r_0, m_0 \rangle$  and  $\langle r'_0, m'_0 \rangle$  such that  $r_0|_{\mathbb{L}} = r'_0|_{\mathbb{L}}$  and  $m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}}$ , and for all number of step  $n$ ,

$$\langle m_0, r_0 \rangle \xrightarrow[\delta']{\delta}^n \langle m_n, r_n \rangle \implies \langle m'_0, r'_0 \rangle \xrightarrow[\delta']{\delta}^n \langle m'_n, r'_n \rangle \wedge o = o' \wedge \delta = \delta'$$

This is the main lemma:

**Lemma 16.** Under Hyp. 1 and 2, for all program  $P$ , number of steps  $n$ , memories  $m_0$  and  $m'_0$ , register maps  $r_0$  and  $r'_0$ , and microarchitectural context  $\mu_0$ ,

$$\begin{aligned}
m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \wedge r_0|_{\mathbb{L}} = r'_0|_{\mathbb{L}} \wedge \langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{n} \langle m_n, r_n, buf_n, \mu_n \rangle &\implies \\
\langle m'_0, r'_0, \varepsilon, \mu_0 \rangle \xrightarrow{n} \langle m'_n, r'_n, buf'_n, \mu'_n \rangle \wedge & \text{(Gstepn)} \\
\lfloor buf_n \rfloor_{\mathbb{L}} = \lfloor buf'_n \rfloor_{\mathbb{L}} \wedge & \text{(Gbuf)} \\
\|r_n\|_{\mathbb{L}} = \|r'_n\|_{\mathbb{L}} \wedge & \text{(Greg)} \\
m_n|_{\mathbb{L}} = m'_n|_{\mathbb{L}} \wedge & \text{(Gmem)} \\
\mu_n = \mu'_n \wedge & \text{(Gmicro)} \\
corr_{\vec{\alpha}, \vec{c}}(n) = corr_{\vec{\alpha}', \vec{c}'}(n) \wedge & \text{(Gcorr)} \\
\forall 0 \leq i \leq |buf_n|. \text{transient}(\langle m_n, r_n, buf_n[0..i], - \rangle) = \text{transient}(\langle m'_n, r'_n, buf'_n[0..i], - \rangle) & \text{(Gtrans)}
\end{aligned}$$

where  $\vec{\alpha}$  and  $\vec{\alpha}'$  are the longest sequential runs, respectively starting from  $\langle m_0, r_0 \rangle$  and  $\langle m'_0, r'_0 \rangle$ ; and  $\vec{c}$  and  $\vec{c}'$  are the longest PROSPECT runs, respectively starting from  $\langle m_0, r_0, \varepsilon, \mu \rangle$  and  $\langle m'_0, r'_0, \varepsilon, \mu \rangle$ .

*Proof.* Assume a program  $P$  satisfying Hyp. 2, memories  $m_0$  and  $m'_0$ , register maps  $r_0$  and  $r'_0$ , and a microarchitectural context  $\mu_0$ , such that:

$$\begin{aligned}
m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \text{ and } r_0|_{\mathbb{L}} = r'_0|_{\mathbb{L}} & \text{(Hloweq)} \\
\langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{n} \langle m_n, r_n, buf_n, \mu_n \rangle & \text{(Hstepn)}
\end{aligned}$$

Under these hypothesis, we show that (Gstepn), (Gbuf), (Gmem), (Gmicro), (Gcorr), and (Gtrans). The proof goes by induction on the number of steps  $n$ .

**Base case ( $n = 0$ ):**

- (Gstepn)  $\langle m'_0, r'_0, buf'_0, \mu'_0 \rangle \xrightarrow{0} \langle m'_0, r'_0, buf'_0, \mu'_0 \rangle$
- (Gbuf)  $\lfloor buf_0 \rfloor_{\mathbb{L}} = \lfloor buf'_0 \rfloor_{\mathbb{L}} = \varepsilon$
- (Greg)  $\|r_0\|_{\mathbb{L}} = \|r'_0\|_{\mathbb{L}}$  follows from the application of Corollary 4 with (Hloweq) and Lemma 3,
- (Gmem)  $m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}}$  directly follows from (Hloweq),
- (Gmicro)  $\mu_0 = \mu'_0$  because the initial microarchitectural context is the same in both initial configurations,
- (Gcorr)  $corr_{\vec{\alpha}, \vec{c}}(0) = corr_{\vec{\alpha}', \vec{c}'}(0) = \{0 \mapsto 0\}$  by Definition 19,
- (Gtrans)  $\forall 0 \leq i \leq |buf_0|. \text{transient}(\langle m_0, r_0, buf_0[0..i], \mu_0 \rangle) = \text{transient}(\langle m'_0, r'_0, buf'_0[0..i], \mu'_0 \rangle)$  follows directly by definition of *transient* (cf. Definition 17) and  $buf_0 = buf'_0 = \varepsilon$ .

**Inductive case:** We assume that Lemma 16 holds at step  $n - 1$ , meaning that:

$$\begin{aligned}
\langle m'_0, r'_0, \varepsilon, \mu_0 \rangle \xrightarrow{n-1} \langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle & \text{(IHstepn)} \\
\|buf_{n-1}\|_{\mathbb{L}} = \|buf'_{n-1}\|_{\mathbb{L}} & \text{(IHbuf)} \\
\|r_{n-1}\|_{\mathbb{L}} = \|r'_{n-1}\|_{\mathbb{L}} & \text{(IHreg)} \\
m_{n-1}|_{\mathbb{L}} = m'_{n-1}|_{\mathbb{L}} & \text{(IHmem)} \\
\mu_{n-1} = \mu'_{n-1} & \text{(IHmicro)} \\
corr_{\vec{\alpha}, \vec{c}}(n-1) = corr_{\vec{\alpha}', \vec{c}'}(n-1) & \text{(IHcorr)} \\
\forall 0 \leq i \leq |buf_{n-1}|. \text{transient}(\langle m_{n-1}, r_{n-1}, buf_{n-1}[0..i], - \rangle) = \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}[0..i], - \rangle) & \text{(IHtrans)}
\end{aligned}$$

Under these hypotheses, we show that Lemma 16 still holds at step  $n$ .

**Simplify goal (Gstepn):** Notice that by Definition 10 and (Hstepn), we have that:

$$\langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle \xrightarrow{1} \langle m_n, r_n, buf_n, \mu_n \rangle \text{ (IHstep)}$$

which together with (Hloweq), gives us that (IHstepn), (IHbuf), (IHreg) (IHmem) and (IHmicro) hold at step  $n - 1$ . Additionally, from Definition 10 and (IHstepn), proving (Gstepn) amounts to show:

$$\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle \rightarrow \langle m'_n, r'_n, buf'_n, \mu'_n \rangle \quad (\text{Gstep})$$

Consequently, we have to show that (Gstep), (Gbuf), (Greg) (Gmem), (Gmicro), (Gcorr) and (Gtrans) hold at step  $n$ .

**Transform (IHcorr):** First, observe that because the semantics is deterministic (cf Hyp. 1), we have that:

$$\vec{c}_{n-1} = \langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle \text{ and } \vec{c}'_{n-1} = \langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle \quad (\text{H}\vec{c}_{n-1})$$

From this, Lemma 5 and (IHcorr), we have that for all  $buf \in \text{prefix}(buf_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$  and  $buf' \in \text{prefix}(buf'_{n-1}, \langle m'_{n-1}, r'_{n-1} \rangle)$  such that  $|buf| = |buf'|$ ,

$$\langle m_{n-1}, r_{n-1} \rangle \uplus buf = \alpha_j \text{ and } \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf' = \alpha'_j \text{ where } j = \text{corr}_{\vec{\alpha}, \vec{c}}(n-1)(|buf|) \quad (\text{IHarch})$$

**Step rule:** The step rule updates the microarchitectural context such that:

$$\begin{aligned} \mu_{aux} &\triangleq \text{update}(\mu_{n-1}, m_{n-1} |_{\text{L}}, r_{n-1} |_{\text{L}}, [buf_{n-1}]_{\text{L}}) \\ \mu'_{aux} &\triangleq \text{update}(\mu'_{n-1}, m'_{n-1} |_{\text{L}}, r'_{n-1} |_{\text{L}}, [buf'_{n-1}]_{\text{L}}) \end{aligned}$$

We start by showing that  $\mu_{aux} = \mu'_{aux}$ . Because *update* is deterministic, this follows from:

- $\mu_{n-1} = \mu'_{n-1}$ , which directly follows from (IHmicro),
- $m_{n-1} |_{\text{L}} = m'_{n-1} |_{\text{L}}$ , which directly follows from (IHmem),
- $r_{n-1} |_{\text{L}} = r'_{n-1} |_{\text{L}}$ , which follows from (IHreg), Corollary 4 and Lemma 3,
- $[buf_{n-1}]_{\text{L}} = [buf'_{n-1}]_{\text{L}}$ , which follows from (IHbuf) and Lemma 8.

Next, the rule chooses a directive and applies the corresponding evaluation rule on the current configuration. By (IHstep), in the first configuration, the rule selects a directive  $d \triangleq \text{next}(\mu_{aux})$  and updates the current configuration such that:

$$\langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{aux} \rangle \xrightarrow{d} \langle m_n, r_n, buf_n, \mu_n \rangle$$

We show that in the second configuration, the STEP rule also applies the same directive  $d$ .

In the second configuration, the next directive to apply is  $d' \triangleq \text{next}(\mu'_{aux})$ . By  $\mu_{aux} = \mu'_{aux}$  and because *next* is deterministic (from Hyp. 1), we have  $d = d'$  which means that both configurations evaluate the same directive at step  $n - 1$ .

**Proof of (Gcorr):** Observe that to show (Gcorr), we have to show that  $\text{corr}_{\vec{\alpha}, \vec{c}}(n) = \text{corr}_{\vec{\alpha}', \vec{c}'}(n)$ . By (H\vec{c}\_{n-1}) and Definition 19, this follows from (IHcorr) and the following conditions:

1.  $\text{next}(\mu_{aux}) = \text{next}(\mu'_{aux})$ , which we have just shown;
2.  $\text{transient}(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle) \iff \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle)$ , which directly follows from  $|buf_{n-1}| = |buf'_{n-1}|$  (by Definition 21 and (IHbuf)) and (IHtrans);
3. In the case  $d = \text{fetch}$ , we additionally have to show

$$\neg \text{transient}(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle) \implies \text{lst\_pc}(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle) = \text{lst\_pc}(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \_ \rangle)$$

In other words, assuming  $\neg \text{transient}(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle)$ , we need to show that  $r_{seq}(\text{pc}) = r'_{seq}(\text{pc})$  where  $\langle \cdot, r_{seq} \rangle = \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}$  and  $\langle \cdot, r'_{seq} \rangle = \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1}$ . From Lemma 4, we can instead show that  $\text{apl}(buf_{n-1}, r_{n-1})(\text{pc}) = \text{apl}(buf'_{n-1}, r'_{n-1})(\text{pc})$ . From the application of Lemma 12 with (IHreg) and (IHbuf), we have  $\|\text{apl}(buf_{n-1}, r_{n-1})\|_{\text{L}} = \|\text{apl}(buf'_{n-1}, r'_{n-1})\|_{\text{L}}$ , meaning that  $\|\text{apl}(buf_{n-1}, r_{n-1})(\text{pc})\|_{\text{L}} = \|\text{apl}(buf'_{n-1}, r'_{n-1})(\text{pc})\|_{\text{L}}$ . Finally, because the security level of  $\text{pc}$  is L (cf. Corollary 1) we have from Lemma 11 that the security level of  $\text{apl}(buf_{n-1}, r_{n-1})(\text{pc})$  and  $\text{apl}(buf'_{n-1}, r'_{n-1})(\text{pc})$  is also L, which by  $\|\text{apl}(buf_{n-1}, r_{n-1})(\text{pc})\|_{\text{L}} = \|\text{apl}(buf'_{n-1}, r'_{n-1})(\text{pc})\|_{\text{L}}$  means  $\text{apl}(buf_{n-1}, r_{n-1})(\text{pc}) = \text{apl}(buf'_{n-1}, r'_{n-1})(\text{pc})$ . This concludes the proof that  $r_{seq}(\text{pc}) = r'_{seq}(\text{pc})$ .

This concludes the proof of **(Gcorr)**.

Knowing that the directive that is applied is the same in both configurations, we can proceed to show the remaining goals by case analysis on the directive  $d$ . We consider the hardware evaluation rules for the directives `fetch`, `execute  $i$` , and `retire`. For simplicity, we rename  $\mu_{aux}$  and  $\mu'_{aux}$  as  $\mu_{n-1}$  and  $\mu'_{n-1}$  respectively and, because  $\mu_{aux} = \mu'_{aux}$ , we let **(IHmicro)** denote the equality of these renamed architectural states.

**Fetch directive.** All `FETCH` rules (cf. Fig. 4), start by evaluating the value of `pc` to get the current location using respectively  $apl(buf_{n-1}, r_{n-1})$  and  $apl(buf'_{n-1}, r'_{n-1})$ . From the application of Lemma 12 with **(IHreg)** and **(IHbuf)**, we have:

$$\|apl(buf_{n-1}, r_{n-1})\|_L = \|apl(buf'_{n-1}, r'_{n-1})\|_L \quad (\text{Hapl})$$

The goal now is to show that both executions evaluate `pc` to the same value. From **(IHstep)**, we know that the evaluation of the expressions do not get stuck in the first configuration. Hence from Lemma 15, and **(Hapl)**, we know that it is not stuck in the second configuration either. Hence the values of `pc` in both configurations is respectively given by:

$$(1:s) \triangleq \llbracket pc \rrbracket_{apl(buf_{n-1}, r_{n-1})} \quad \text{and} \quad (1':s') \triangleq \llbracket pc \rrbracket_{apl(buf'_{n-1}, r'_{n-1})}$$

From the expression evaluation rules (cf. Fig. 3), we have:

$$(1:s) = apl(buf_{n-1}, r_{n-1})(pc) \quad \text{and} \quad (1':s') = apl(buf'_{n-1}, r'_{n-1})(pc)$$

Additionally, from **(Hapl)**, we have  $\|(1:s)\|_L = \|(1':s')\|_L$ . Finally, from Corollary 1 and Lemma 11, we have  $s = s' = L$ , meaning that  $1 = 1'$ .

**(Gstep)** In all `FETCH` rules the only hypothesis that can block the execution is if the evaluation of expression is stuck. However, we have shown that, from **(Hapl)** and **(IHstep)** and Lemma 15, the expression evaluation in the second rule is not stuck, which entails **(Gstep)**.

**(Greg)**, **(Gmem)**, and **(Gmicro)**: Because the register map, the memory, and the microarchitectural context are not updated in any of the `FETCH` rules, **(Greg)**, **(Gmem)**, and **(Gmicro)** directly follow from **(IHreg)**, **(IHmem)**, and **(IHmicro)**.

**(Gbuf)**, **(Gtrans)**: Because both configurations evaluate `pc` to the same value  $1$  and fetch the same instruction (i.e., the instruction at  $P[1]$ ), then they either both evaluate `FETCH-PREDICT-BRANCH-JMP` or they both evaluate `FETCH-OTHERS`. We show the remaining goals **(Gbuf)** and **(Gtrans)** separately for each `FETCH` rule:

`FETCH-PREDICT-BRANCH-JMP`: An instruction that moves control to the next target is added to the buffer such that:

$$buf_n = buf_{n-1} \cdot pc \leftarrow (1_n:L) @ 1 \quad \text{and} \quad buf'_n = buf'_{n-1} \cdot pc \leftarrow (1'_n:L) @ 1'$$

where  $1_n = predict(\mu_{n-1})$  and  $1'_n = predict(\mu'_{n-1})$ .

To show **(Gbuf)**, we have to show that  $\lfloor buf_n \rfloor_L = \lfloor buf'_n \rfloor_L$ , which from Definition 9 and **(IHbuf)**, amounts to that  $\lfloor pc \leftarrow (1_n:L) @ 1 \rfloor_L = \lfloor pc \leftarrow (1'_n:L) @ 1' \rfloor_L$ . We have already shown that  $1 = 1'$ . Hence it just remains to show  $1_n = 1'_n$  which directly follows from **(IHmicro)** and Hyp. 1.

To show **(Gtrans)**, by **(IHtrans)**, the definition of *transient* in Definition 17, and the definition of  $buf_n$  and  $buf'_n$ , we simply need to show  $transient(\langle m_n, r_n, buf_n, \mu_n \rangle) \iff transient(\langle m'_n, r'_n, buf'_n, \mu'_n \rangle)$ . We first consider the case where  $transient(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle) = true$  and then the case where  $transient(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle) = false$ .

- In the case,  $transient(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle) = true$ , by **(IHtrans)** we also have  $transient(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \_ \rangle) = true$ . By definition of *transient* (cf. Definition 19),  $buf_n$  and  $buf'_n$  we also have  $transient(\langle m_n, r_n, buf_n, \_ \rangle) = transient(\langle m'_n, r'_n, buf'_n, \_ \rangle) = true$ ;
- In the case,  $transient(\langle m_{n-1}, r_{n-1}, buf_{n-1}, \_ \rangle) = false$ , by **(IHtrans)** we also have  $transient(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \_ \rangle) = false$ . By definition of *transient* (cf. Definition 17),  $buf_n$  and  $buf'_n$  and by  $m_{n-1} = m_n$ ,  $m'_{n-1} = m'_n$  and  $r_{n-1} = r_n$ ,  $r'_{n-1} = r'_n$  we have to show:

$$goodpred(pc \leftarrow (1_n:L) @ 1, \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}) \iff goodpred(pc \leftarrow (1_n:L) @ 1, \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1})$$

We focus on the case where the fetched instruction  $P[1] = \mathbf{beqz} \ e \ 1_{br}$  (the case  $P[1] = \mathbf{jmp} \ e$  is similar). From the definition of *goodpred* (cf. Definition 17), this amounts to showing  $\llbracket e \rrbracket_{r_{seq}} = 0 \iff \llbracket e \rrbracket_{r'_{seq}} = 0$  where  $r_{seq} = \langle m_{n-1}, r_{n-1} \rangle \uplus$



$buf_{n-1}$  and  $r'_{seq} = \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1}$ . Notice that because there are no mispredicted instructions in  $buf_{n-1}$  and  $buf'_{n-1}$  and because reorder buffers are well-formed (Lemma 2), we have  $buf_{n-1} \in \text{prefix}(buf'_{n-1})$  and  $buf'_{n-1} \in \text{prefix}(buf_{n-1})$ . By (IHArch), and because  $|buf_{n-1}| = |buf'_{n-1}|$  we get that  $\langle \_, r_{seq} \rangle = \alpha_j$  and  $\langle \_, r'_{seq} \rangle = \alpha'_j$  where  $j = \text{corr}_{\bar{a}, \bar{c}}(n-1)(|buf_{n-1}|)$ . From Corollary 2, and the definition of  $\mathbb{1}$ , we know that  $\llbracket pc \rrbracket_{r_{seq}} = \llbracket pc \rrbracket_{r'_{seq}} = \mathbb{1}$ . Hence, because  $P[\mathbb{1}] = \mathbf{beqz} \ e \ \mathbb{1}_{\text{br}}$ , we know that we can apply the BRANCH rule from the sequential semantics (Fig. 8) to  $\alpha_j$  and  $\alpha'_j$ . Consequently, we have  $\alpha_j \rightsquigarrow_{\bar{o}} \_$  and  $\alpha'_j \rightsquigarrow_{\bar{o}'} \_$  where  $\bar{o} = (\llbracket e \rrbracket_{r_{seq}} = 0)$  and  $\bar{o}' = (\llbracket e \rrbracket_{r'_{seq}} = 0)$ . Moreover, because the program is constant-time Hyp. 2, we have  $\bar{o} = \bar{o}'$ , which concludes  $\llbracket e \rrbracket_{r_{seq}} = 0 \iff \llbracket e \rrbracket_{r'_{seq}} = 0$  and, in turn,  $\text{transient}(\langle m_n, r_n, buf_n \rangle) \iff \text{transient}(\langle m'_n, r'_n, buf'_n \rangle)$ .

FETCH-OTHERS: In the rule FETCH-OTHERS, two instructions are added to the buffer:

$$\begin{aligned} buf_n &= buf_{n-1} \cdot P[\mathbb{1}]@ \varepsilon \cdot pc \leftarrow (\mathbb{1}_n : L) @ \varepsilon \\ buf'_n &= buf'_{n-1} \cdot P[\mathbb{1}']@ \varepsilon \cdot pc \leftarrow (\mathbb{1}'_n : L) @ \varepsilon \end{aligned}$$

where  $\mathbb{1}_n = \llbracket pc + 1 \rrbracket_{apl(r_{n-1}, buf_{n-1})}$  and  $\mathbb{1}'_n = \llbracket pc + 1 \rrbracket_{apl(r'_{n-1}, buf'_{n-1})}$ . We have already shown that  $\mathbb{1} = \mathbb{1}'$ . In the same way, we can show that  $\mathbb{1}_n = \mathbb{1}'_n$ . Consequently, the same instructions are added to the reorder buffers in both executions. Therefore, (Gbuf) follows from Definition 21 and (IHbuf). Additionally, because the register map and memory are not modified and because instructions added to the buffer have tag  $\varepsilon$ , (Gtrans), follows directly from (IHtrans).

This concludes the proof for the fetch directive.

**Execute  $i$ .** From (IHstep), we can apply an EXECUTE directive with an index  $i$  in the first configuration. Consequently, we have that:

$$buf_{n-1} = buf_a \cdot inst @ T \cdot buf_b \text{ such that } |buf_a| = i - 1$$

From (IHbuf) and Definition 21, there is also a  $i^{\text{th}}$  instruction  $inst'$  in  $buf'_{n-1}$  such that:  $buf'_{n-1} = buf'_a \cdot inst' @ T' \cdot buf'_b$ . Additionally we have:

$$\begin{aligned} \llbracket buf_a \rrbracket_L &= \llbracket buf'_a \rrbracket_L && \text{(Hbufa)} \\ \llbracket inst @ T \rrbracket_L &= \llbracket inst' @ T' \rrbracket_L && \text{(Hinst)} \\ \llbracket buf_b \rrbracket_L &= \llbracket buf'_b \rrbracket_L && \text{(Hbufb)} \end{aligned}$$

From the application of Lemma 13 with (Hbufa), (IHreg) we also have:

$$\llbracket aplsan(buf_a, r_{n-1}) \rrbracket_L = \llbracket aplsan(buf'_a, r'_{n-1}) \rrbracket_L \quad \text{(Haplsan)}$$

and from the application of Lemma 12 with (Hbufa), (IHreg) we have:

$$\llbracket apl(buf_a, r_{n-1}) \rrbracket_L = \llbracket apl(buf'_a, r'_{n-1}) \rrbracket_L \quad \text{(Hapl)}$$

In all the EXECUTE rules, expressions are evaluated using  $aplsan(buf_a, r_{n-1})$  or  $apl(buf_a, r_{n-1})$  in the first execution or  $aplsan(buf'_a, r'_{n-1})$  or  $apl(buf'_a, r'_{n-1})$ . From (IHstep), we know that the evaluation of expressions is not stuck in the first execution. Therefore, from the application of Lemma 15 with (Haplsan) and (Hapl), we know that:

$$\text{The evaluation of expressions does not get stuck in the second configuration.} \quad \text{(Hexpr)}$$

In all the EXECUTE rules, the memory and the reorder buffer are not modified. Therefore, (Greg) and (Gmem) directly follow from induction hypotheses (IHreg) and (IHmem). We show the remaining goals (Gstep), (Gbuf), (Gmicro), and (Gtrans) for each EXECUTE rule.

BRANCH-COMMIT and BRANCH-ROLLBACK: From the hypotheses of the rule, the instruction  $inst @ T$  that is executed in the first configuration is  $pc \leftarrow (\mathbb{1} : \_) @ \mathbb{1}_0$ . From (Hinst) and Definition 21, we have that  $inst' @ T' = pc \leftarrow (\mathbb{1}' : \_) @ \mathbb{1}_0$ . Additionally, from Corollary 1 and (Hinst), we have

$$\mathbb{1} = \mathbb{1}' \quad \text{(Hloc)}$$

Moreover, considering that the first execution evaluates either BRANCH-COMMIT or BRANCH-ROLLBACK, we have  $P[\mathbb{1}_0] = \mathbf{beqz} \ e \ \mathbb{1}_{\text{br}}$ . Therefore, the second configuration can only evaluate the rules BRANCH-COMMIT or BRANCH-ROLLBACK.

The rule computes conditions  $c$  and  $c'$  such that:

$$(c; \_)\triangleq \llbracket e \rrbracket_{\text{aplsan}(buf_a, r_{n-1})} \text{ and } (c'; \_)\triangleq \llbracket e \rrbracket_{\text{aplsan}(buf'_a, r'_{n-1})}$$

We now show that  $(c = 0) \iff (c' = 0)$ . We first consider the case in which both configurations are in sequential execution; and then the case in which both configurations are in speculative execution (note that from (Hbufa) and Lemma 10, other cases are impossible):

1. Both configurations are in sequential execution. In this case, because there are no mispredicted instructions in  $buf_a$  and  $buf'_a$  and because reorder buffers are well-formed (Lemma 2), we have  $buf_a \in \text{prefix}(buf'_{n-1})$  and  $buf'_a \in \text{prefix}(buf_{n-1})$ . Let  $\langle m_a, r_a \rangle = \langle m_{n-1}, r_{n-1} \rangle \uplus buf_a$  and  $\langle m'_a, r'_a \rangle = \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_a$ . By (IHarch), and because  $|buf_a| = |buf'_a| = i - 1$  we get that  $\langle m_a, r_a \rangle = \alpha_j$  and  $\langle m'_a, r'_a \rangle = \alpha'_j$  where  $j = \text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(i-1)$ .

From Definition 16, we know that  $\llbracket pc \rrbracket_{r_a} = \llbracket pc \rrbracket_{r'_a} = 1_0$ . Hence, because  $P[1_0] = \mathbf{beqz} \ e \ 1_{\text{br}}$ , we know that we can apply the BRANCH rule from the sequential semantics (Fig. 8) to  $\alpha_j$  and  $\alpha'_j$ . Consequently, we have  $\alpha_j \rightsquigarrow \_$  and  $\alpha'_j \rightsquigarrow \_$  where  $o = (\llbracket e \rrbracket_{r_a} = 0)$  and  $o' = (\llbracket e \rrbracket_{r'_a} = 0)$ . Moreover, because the program is constant-time Hyp. 2, we have  $o = o'$ . By definition of  $c$  and  $c'$  and by Corollary 3, we have that  $(c; \_) = \llbracket e \rrbracket_{r_a}$  and  $(c'; \_) = \llbracket e \rrbracket_{r'_a}$ . Hence, by  $o = o'$ , we get  $(c = 0) \iff (c' = 0)$ .

2. Both configurations are in speculative execution. In this case, from Definition 5, we have:

$$(c; \_) = \llbracket e \rrbracket_{\text{apl}(buf_a, r_{n-1})|_{\text{L}}} \text{ and } (c'; \_) = \llbracket e \rrbracket_{\text{apl}(buf'_a, r'_{n-1})|_{\text{L}}}$$

From the application of Corollary 5 with (Hapl), we have  $\text{apl}(buf_a, r_{n-1})|_{\text{L}} = \text{apl}(buf'_a, r'_{n-1})|_{\text{L}}$ , which entails  $c = c'$  and concludes  $(c = 0) \iff (c' = 0)$ .

Then, the rule computes the next target, which from  $(c = 0) \iff (c' = 0)$ , is the same in both executions:

$$1_{\text{next}} \triangleq \text{if } c = 0 \text{ then } 1_{\text{br}} \text{ else } 1_0 + 1 \text{ and}$$

From (Hloc), this also means that the condition  $1_{\text{next}} = 1$ , which selects whether BRANCH-COMMIT or BRANCH-ROLLBACK is applied, has the same value in both executions. Hence either both executions evaluate the rule BRANCH-COMMIT or both executions evaluate the rule BRANCH-ROLLBACK.

(Gmicro) The microarchitectural context is not modified by the rules so (Gmicro) directly follows from (IHmicro).

(Gstep) From (Hexpr), we have that the evaluation of expressions is not stuck. The hypotheses  $1_{\text{next}} = 1$  and  $1_{\text{next}} \neq 1$  do not block the execution but just selects which rule is applied: if  $1_{\text{next}} = 1$  the rule BRANCH-COMMIT is applied, otherwise the rule BRANCH-ROLLBACK is applied. Hence in both cases a rule can be applied, which entails (Gstep).

(Gbuf) and (Gtrans). We first consider the case where both executions evaluate the rule BRANCH-COMMIT and then the case where both execution evaluate the rule BRANCH-ROLLBACK (we have shown before that other cases are not possible).

- Case BRANCH-COMMIT: By the hypothesis of the rule and (Hloc), the reorder buffers are updated such that:

$$buf_n = buf_a \cdot pc \leftarrow (1:L) @ \varepsilon \cdot buf_b \text{ and } buf'_n = buf'_a \cdot pc \leftarrow (1:L) @ \varepsilon \cdot buf'_b$$

Therefore, (Gbuf) follows from Definition 21, (Hbufa), (Hbufb) and from  $\llbracket pc \leftarrow (1:L) @ \varepsilon \rrbracket_{\text{L}} = \llbracket pc \leftarrow (1:L) @ \varepsilon \rrbracket_{\text{L}}$ .

Because  $m_{n-1} = m_n$ ,  $m'_{n-1} = m'_n$  and  $r_{n-1} = r_n$ ,  $m_{n-1} = m'_n$ , showing (Gtrans) amounts to showing

$$\forall 0 \leq j \leq |buf_{n-1}|. \text{transient}(\langle m_{n-1}, r_{n-1}, buf_n[0..j], \_ \rangle) = \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf_n[0..j], \_ \rangle) \quad (\text{G})$$

For  $0 \leq j < i$ , (G) follows directly from (IHtrans) and the definition of  $buf_n$  and  $buf'_n$ . For  $j = i$ , (G) follows from the fact that (G) holds for  $0 \leq j < i$  and by the fact that both  $buf_n[i]$  and  $buf'_n[i]$  have tag  $\varepsilon$ . Finally, for  $i < j \leq |buf_n|$ , first notice that by the definition of  $buf_n$  and  $buf'_n$ , by Definition 15 and because the predictions for  $buf_{n-1}[i]$  and  $buf'_{n-1}[i]$  were correct, we have:

$$\begin{aligned} \langle m_{n-1}, r_{n-1} \rangle \uplus buf_n[0..i] &= \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}[0..i] \text{ and} \\ \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_n[0..i] &= \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1}[0..i] \end{aligned}$$

Hence, (G) follows from (IHtrans) and from the fact that (G) holds for  $0 \leq j \leq i$ .

– Case BRANCH-ROLLBACK: By the hypothesis of the rule, the reorder buffers are updated such that:

$$buf_n = buf_a \cdot pc \leftarrow (l_{next}:L) @ \varepsilon \text{ and } buf'_n = buf'_a \cdot pc \leftarrow (l_{next}:L) @ \varepsilon$$

Therefore, (Gbuf) follows from Definition 21, (Hbufa) and from  $\ll pc \leftarrow (l_{next}:L) @ \varepsilon \ll_L = \ll pc \leftarrow (l_{next}:L) @ \varepsilon \ll_L$ .  
The proof for (Gtrans) is similar to the case BRANCH-COMMIT.

JMP-COMMIT and JMP-ROLLBACK: The proof is similar to the case BRANCH-COMMIT and BRANCH-ROLLBACK.

EXECUTE-ASSIGN: From the hypotheses of the rule, the instruction  $inst@T$  that is executed in the first configuration is  $inst = r \leftarrow e@T$  where  $e \notin \hat{\mathcal{V}}$ . From (Hinst) and Definition 21, we have that  $inst'@T' = r \leftarrow e@T$ . Therefore, the second configuration can only evaluate the rule EXECUTE-ASSIGN.

The rule evaluates the expression  $e$  to values  $v$  (in the first configuration) and  $v'$  (in the second configuration) such that:

$$(v:s) \triangleq \ll e \ll_{apl(buf_a, r_{n-1})} \text{ and } (v':s') \triangleq \ll e \ll_{apl(buf'_a, r'_{n-1})}$$

From (Hapl), and Lemma 15 we have that  $\ll (v:s) \ll_L = \ll (v':s') \ll_L$ .

(Gmicro) The microarchitectural context is not modified by the rule so (Gmicro) directly follows from (IHmicro).

(Gstep) The first hypothesis that can block the execution in the second configuration is  $e \notin \hat{\mathcal{V}}$ . We have show that  $e$  is the same in both executions and from (IHstep) we have  $e \notin \hat{\mathcal{V}}$ . The second hypothesis that can block the execution in the second configuration is if the evaluation of the expression gets stuck. From (Hexpr), we know that it does not get stuck. Hence the rule EXECUTE-ASSIGN can also be applied in the second configuration, which entails (Gstep).

(Gbuf) The reorder buffers are updated such that:

$$buf_n = buf_a \cdot r \leftarrow (v:s) \cdot buf_b \text{ and } buf'_n = buf'_a \cdot r \leftarrow (v':s') \cdot buf'_b$$

From (Hbufa), (Hbufb), and Definition 20, we only need to show  $\ll r \leftarrow (v:s) \ll_L = \ll r \leftarrow (v':s') \ll_L$ , which amounts to show  $\ll (v:s) \ll_L = \ll (v':s') \ll_L$ . This directly follows from the application of Lemma 9 with  $\ll (v:s) \ll_L = \ll (v':s') \ll_L$ .

(Gtrans) Because  $m_{n-1} = m_n$ ,  $m'_{n-1} = m'_n$  and  $r_{n-1} = r_n$   $m_{n-1} = m'_n$ , showing (Gtrans) amounts to showing

$$\forall 0 \leq j \leq |buf_{n-1}|. \text{transient}(\langle m_{n-1}, r_{n-1}, buf_n[0..j], \_ \rangle) = \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf_n[0..j], \_ \rangle) \quad (G)$$

Notice that from by the definition of  $buf_n$  and  $buf'_n$ , and by Definition 15, we have:

$$\begin{aligned} \langle m_{n-1}, r_{n-1} \rangle \uplus buf_n[0..i] &= \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}[0..i] \text{ and} \\ \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_n[0..i] &= \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1}[0..i] \end{aligned}$$

Hence, because no other instructions are modified in the ROB, (G) follows from (IHtrans).

EXECUTE-LOAD-PREDICT: From the hypotheses of the rule, the instruction  $inst@T$  that is executed in the first configuration is  $inst@T = x \leftarrow \mathbf{load} e@T$ . From (Hinst) and Definition 21, we have that  $inst'@T' = x \leftarrow \mathbf{load} e@T$ . Therefore, the second configuration can only evaluate the rule EXECUTE-LOAD-PREDICT.

(Gmicro) The microarchitectural context is not modified by the rule so (Gmicro) directly follows from (IHmicro).

(Gstep) From (Hexpr), we have that the evaluation of expressions is not stuck. Because no other hypothesis can block the evaluation of the rule, it can also be applied in the second configuration, which entails (Gstep).

(Gbuf) The reorder buffers are updated such that:

$$buf_n = buf_a \cdot x \leftarrow (v:L) @ 1 \cdot buf_b \text{ and } buf'_n = buf'_a \cdot x \leftarrow (v':L) @ 1' \cdot buf'_b$$

where

$$\begin{aligned} v &= \text{predict}(\mu_{n-1}) \text{ and } v' = \text{predict}(\mu'_{n-1}) \\ (1:s) &= \ll pc \ll_{apl(buf_a, r_{n-1})} \text{ and } (1':s') = \ll pc \ll_{apl(buf'_a, r'_{n-1})} \end{aligned}$$

From (Hbufa), (Hbufb), and Definition 21, we only need to show  $\ll x \leftarrow (v:L) @ 1 \ll_L = \ll x \leftarrow (v':L) @ 1' \ll_L$  which amounts to showing  $v = v'$  and  $1 = 1'$ .

- $v = v'$  follows from the fact that *predict* is deterministic (cf. Hyp. 1) and (IHmicro).
- From the expression evaluation rules (cf. Fig. 3), we have:

$$(1:s) = \text{apl}(buf_a, r_{n-1})(pc) \text{ and } (1':s') = \text{apl}(buf'_a, r'_{n-1})(pc)$$

Additionally, from (Hapl) we have  $\|(1:s)\|_L = \|(1':s')\|_L$ . Finally, from Corollary 1 and Lemma 11, we have  $s = s' = L$ , meaning that  $1 = 1'$ .

(Gtrans) Because  $m_{n-1} = m_n$ ,  $m'_{n-1} = m'_n$  and  $r_{n-1} = r_n$ ,  $m_{n-1} = m'_{n-1}$ , and by definition of *transient* (cf. Definition 17) showing (Gtrans) amounts to showing for all  $j$  such that  $0 \leq j \leq |buf_{n-1}|$ ,

$$\forall 0 \leq j \leq |buf_{n-1}|. \text{transient}(\langle m_{n-1}, r_{n-1}, buf_n[0..j], \_ \rangle) = \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf_n[0..j], \_ \rangle) \quad (\text{G})$$

For  $0 \leq j < i$ , (G) follows directly from  $buf_n[0..i-1] = buf_{n-1}[0..i-1]$ ,  $buf'_n[0..i-1] = buf'_{n-1}[0..i-1]$  and (IHtrans). For  $j \geq i$ , we consider two cases separately. First the case where  $\text{transient}(m_{n-1}, r_{n-1}, buf_n[0..i-1])$  and second, the case where  $\neg \text{transient}(m_{n-1}, r_{n-1}, buf_n[0..i-1])$ .

- In case  $\text{transient}(m_{n-1}, r_{n-1}, buf_n[0..i-1])$ , we also have  $\text{transient}(m'_{n-1}, r'_{n-1}, buf'_n[0..i-1])$  from  $buf_n[0..i-1] = buf_{n-1}[0..i-1]$ ,  $buf'_n[0..i-1] = buf'_{n-1}[0..i-1]$  and (IHtrans). This in turns implies  $\text{transient}(m_{n-1}, r_{n-1}, buf_n[0..j])$  and  $\text{transient}(m'_{n-1}, r'_{n-1}, buf'_n[0..j])$ , which concludes (G);
- In case  $\neg \text{transient}(m_{n-1}, r_{n-1}, buf_n[0..i-1])$ , we also have  $\neg \text{transient}(m'_{n-1}, r'_{n-1}, buf'_n[0..i-1])$  from  $buf_n[0..i-1] = buf_{n-1}[0..i-1]$ ,  $buf'_n[0..i-1] = buf'_{n-1}[0..i-1]$  and (IHtrans).

Let us first focus on  $j = i$ . By definition of *transient* (cf. Definition 17), and because (G) holds for  $j < i$ , we simply have to show:

$$\text{goodpred}(pc \leftarrow (1_n:L) @ 1, \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}) \iff \text{goodpred}(pc \leftarrow (1_n:L) @ 1, \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1})$$

From the definition of *goodpred* (cf. Definition 17), this amounts to showing

$$\llbracket e \rrbracket_{r_{j-1}} = a \wedge s_m(a) = L \wedge m(a) = v \iff \llbracket e \rrbracket_{r'_{j-1}} = a' \wedge s_m(a') = L \wedge m'(a') = v$$

with  $r_{j-1} = \langle m_{n-1}, r_{n-1} \rangle \uplus buf_n[0..j-1]$  and  $r'_{j-1} = \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_n[0..j-1]$ . Notice that because there are no mispredicted instructions in  $buf_n[0..j-1]$  and  $buf'_n[0..j-1]$  and because reorder buffers are well-formed (Lemma 2), we have  $buf_n[0..j-1] \in \text{prefix}(buf'_{n-1})$  and  $buf'_n[0..j-1] \in \text{prefix}(buf_{n-1})$ . By (IHarch), and because  $|buf_n[0..j-1]| = |buf'_n[0..j-1]| = j-1$  we get that  $\langle m_{n-1}, r_{n-1} \rangle = \alpha_j$  and  $\langle m'_{n-1}, r'_{n-1} \rangle = \alpha'_j$  where  $j = \text{corr}_{\bar{\alpha}, \bar{\alpha}'}(n-1)(j-1)$ .

From Corollary 2, and the definition of 1, we know that  $\llbracket pc \rrbracket_{r_{j-1}} = \llbracket pc \rrbracket_{r'_{j-1}} = 1$ . Hence, because  $P[1] = x \leftarrow \text{load } e$ , we know that we can apply the LOAD rule from the sequential semantics (Fig. 8) to  $\alpha_j$  and  $\alpha'_j$ . Consequently, we

have  $\alpha_j \rightsquigarrow_o \_$  and  $\alpha'_j \rightsquigarrow_{o'} \_$  where  $o = a$  and  $o' = a'$ . Moreover, because the program is constant-time Hyp. 2, we have  $a = a'$ . This, in turns, implies  $s_m(a) = L \iff s_m(a') = L$  and if  $s_m(a) = L$ , we get  $m(a) = m'(a')$  from (IHmem) which concludes  $m(a) = v \iff m'(a') = v$ . This concludes (G) for  $j = i$ .

For  $i < j \leq |buf_n|$ , we get by the definition of  $buf_n$  and  $buf'_n$ , and by Definition 15 that

$$\begin{aligned} \langle m_{n-1}, r_{n-1} \rangle \uplus buf_n[0..i] &= \langle m_{n-1}, r_{n-1} \rangle \uplus buf_{n-1}[0..i] \text{ and} \\ \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_n[0..i] &= \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_{n-1}[0..i] \end{aligned}$$

Hence, (G) follows from (IHtrans) and from the fact that (G) holds for  $0 \leq j \leq i$ .

EXECUTE-LOAD-COMMIT and EXECUTE-LOAD-ROLLBACK: From the hypotheses of the rule, the instruction that is executed in the first configuration is  $inst = x \leftarrow (v:\_) @ 1_o$ . From (IHbuf) and Definition 21, we have that  $inst = x \leftarrow (v':\_) @ 1_o$ . Therefore, the second configuration can only evaluate one of the rules EXECUTE-LOAD-COMMIT or EXECUTE-LOAD-ROLLBACK.

From the hypothesis  $P[1_o] = x \leftarrow \text{load } e$ , both rules evaluate the expression  $e$  to values  $a$  (in the first configuration) and  $a'$  (in the second configuration) such that:

$$(a:s) \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf_a, r_{n-1})} \text{ and } (a':s') \triangleq \llbracket e \rrbracket_{\text{aplsan}(buf'_a, r'_{n-1})}$$

We now show that the index of the load is the same in both configurations:

$$\mathbf{a} = \mathbf{a}' \quad (\text{Ha})$$

To show this, we first consider the case in which both configurations are in sequential execution; and then the case in which both configurations are in speculative execution (note that from (Hbufa) and Lemma 10, other cases are impossible):

1. Both configurations are in sequential execution. In this case, because there are no mispredicted instructions in  $buf_a$  and  $buf'_a$  and because reorder buffers are well-formed (Lemma 2), we have  $buf_a \in \text{prefix}(buf'_{n-1})$  and  $buf'_a \in \text{prefix}(buf_{n-1})$ . Let  $\langle m_a, r_a \rangle = \langle m_{n-1}, r_{n-1} \rangle \uplus buf_a$  and  $\langle m'_a, r'_a \rangle = \langle m'_{n-1}, r'_{n-1} \rangle \uplus buf'_a$ . By (IHarch), and because  $|buf_a| = |buf'_a| = i - 1$  we get that  $\langle m_a, r_a \rangle = \alpha_j$  and  $\langle m'_a, r'_a \rangle = \alpha'_j$  where  $j = \text{corr}_{\bar{\alpha}, \bar{c}}(n-1)(i-1)$ .

From Definition 16, we know that  $\llbracket pc \rrbracket_{r_a} = \llbracket pc \rrbracket_{r'_a} = l_0$ . Hence, because  $P[l_0] = x \leftarrow \mathbf{load} \ e$ , we know that we can apply the LOAD rule from the sequential semantics (Fig. 8) to  $\alpha_j$  and  $\alpha'_j$ . Consequently, we have  $\alpha_j \rightsquigarrow_o \_$  and  $\alpha'_j \rightsquigarrow_{o'} \_$  where  $o = \llbracket e \rrbracket_{r_a}$  and  $o' = \llbracket e \rrbracket_{r'_a}$ . Moreover, because the program is constant-time Hyp. 2, we have  $o = o'$ . By definition of  $\mathbf{a}$  and  $\mathbf{a}'$  and by Corollary 3, we have that  $(\mathbf{a}; \_ ) = \llbracket e \rrbracket_{r_a}$  and  $(\mathbf{a}'; \_ ) = \llbracket e \rrbracket_{r'_a}$ . Hence, by  $o = o'$ , we get  $\mathbf{a} = \mathbf{a}'$ .

2. Both configurations are in speculative execution: from Definition 5, we have  $(\mathbf{a}; \mathbf{s}) = \llbracket e \rrbracket_{\text{apl}(buf_a, r_{n-1})|_L}$  and  $(\mathbf{a}'; \mathbf{s}') = \llbracket e \rrbracket_{\text{apl}(buf'_a, r'_{n-1})|_L}$ . From the application of Corollary 5 with (Hapl), we have  $\text{apl}(buf_a, r_{n-1})|_L = \text{apl}(buf'_a, r'_{n-1})|_L$ , which concludes  $\mathbf{a} = \mathbf{a}'$ .

(Gstep) From (Hexpr), we have that the evaluation of expressions is not stuck. Additionally, from (IHstep), we have  $\mathbf{store} \_ \_ \notin buf_a$ , and from (Hbufa) and Definition 21, we have  $\mathbf{store} \_ \_ \notin buf'_a$ . Hypotheses  $\mathbf{v} = m(\mathbf{a}) \wedge s_m(\mathbf{a}) = L$  (in rule EXECUTE-LOAD-COMMIT) and  $\mathbf{v} \neq m(\mathbf{a}) \vee s_m(\mathbf{a}) = H$  (in rule EXECUTE-LOAD-ROLLBACK) do not block the execution but just select which rule is applied. Finally, in case the rule EXECUTE-LOAD-ROLLBACK is applied, we have from (Hbufb) and Corollary 1 that  $buf_b[1] = buf'_b[1] = pc \leftarrow^* (1:L)@E$ . These conditions are sufficient to make a step in the second execution, which entails (Gstep).

(Gbuf) In the rule EXECUTE-LOAD-COMMIT, the reorder buffers are updated such that:

$$buf_n = buf_a \cdot x \leftarrow (m(\mathbf{a}); s_m(\mathbf{a})) \cdot buf_b \text{ and } buf'_n = buf'_a \cdot x \leftarrow (m'(\mathbf{a}); s_m(\mathbf{a})) \cdot buf'_b$$

whereas in the rule EXECUTE-LOAD-ROLLBACK, younger parts of the reorder buffer  $buf_b$  and  $buf'_b$  are forgotten giving reorder buffers:

$$buf_n = buf_a \cdot x \leftarrow (m(\mathbf{a}); s_m(\mathbf{a})) \cdot buf_b[1] \text{ and } buf'_n = buf'_a \cdot x \leftarrow (m'(\mathbf{a}); s_m(\mathbf{a})) \cdot buf'_b[1]$$

From (Hbufa) and (Hbufb) and Definition 21, it is sufficient to show that:

1. Both configurations evaluate the same rule (either EXECUTE-LOAD-COMMIT or EXECUTE-LOAD-ROLLBACK). By the hypotheses of the rule and (Ha), this amounts to show  $\mathbf{v} = \mathbf{v}'$ . Because  $buf_n$  and  $buf'_n$  are well-formed (cf. Lemma 2) and that the security level of predicted values in well-formed buffers is L, we have  $\mathbf{s} = \mathbf{s}' = L$ . By (Hbufa) and Definition 21, it gives us  $\mathbf{v} = \mathbf{v}'$ ;
2.  $\lfloor x \leftarrow (m(\mathbf{a}); s_m(\mathbf{a})) \rfloor_L = \lfloor (m'(\mathbf{a}); s_m(\mathbf{a})) \rfloor_L$ . This follows from (IHmem) and Definition 21: if  $s_m(\mathbf{a}) = L$  then  $m(\mathbf{a}) = m(\mathbf{a})'$  which concludes our goal. Otherwise  $\lfloor x \leftarrow (m(\mathbf{a}); s_m(\mathbf{a})) \rfloor_L = \lfloor (m'(\mathbf{a}); s_m(\mathbf{a})) \rfloor_L = \blacksquare$ .

(Gmicro) In both rules, the microarchitectural contexts are updated with the index  $\mathbf{a}$  (resp.  $\mathbf{a}'$ ). Therefore, (Gmicro) follows from Hyp. 1, (IHmicro), and (Ha).

(Gtrans) The proof is similar to the proof for the case EXECUTE-BRANCH-PREDICT, EXECUTE-BRANCH-ROLLBACK.

EXECUTE-STORE: From the hypotheses of the rule, the instruction that is executed in the first configuration is  $inst = \mathbf{store} \ e_a \ e_v @ T$  where  $e_a, e_v \notin \hat{\mathcal{V}}$ . From (Hinst) and Definition 21, we have that  $\llbracket inst \rrbracket_L = \mathbf{store} \ e_a \ e_v @ T$ . Therefore, the second configuration can only evaluate the rule EXECUTE-STORE.

The rule EXECUTE-STORE evaluates the expressions  $e_a$  and  $e_v$  to values  $\mathbf{a}, \mathbf{v}$  (in the first configuration) and  $\mathbf{a}', \mathbf{v}'$  (in the second configuration):

$$\begin{aligned} (\mathbf{a}; \_ ) &\triangleq \llbracket e_a \rrbracket_{\text{aplsan}(buf_a, r_{n-1})} \text{ and } (\mathbf{a}'; \_ ) \triangleq \llbracket e_a \rrbracket_{\text{aplsan}(buf'_a, r'_{n-1})} \\ (\mathbf{v}; \mathbf{s}) &\triangleq \llbracket e_v \rrbracket_{\text{apl}(buf_a, r_{n-1})} \text{ and } (\mathbf{v}'; \mathbf{s}') \triangleq \llbracket e_v \rrbracket_{\text{apl}(buf'_a, r'_{n-1})} \end{aligned}$$



(Gmicro) The microarchitectural context is not modified by the rule so (Gmicro) directly follows from (IHmicro).

(Gstep) From (Hexpr), we have that the evaluation of expressions is not stuck. Because no other hypothesis can block the evaluation of the rule, it can also be applied in the second configuration, which entails (Gstep).

(Gbuf) The reorder buffers are updated such that:

$$\begin{aligned} buf_n &= buf_a \cdot \mathbf{store} (a:L) (v:s) \cdot buf_b \text{ and} \\ buf'_n &= buf'_a \cdot \mathbf{store} (a':L) (v':s') \cdot buf'_b \end{aligned}$$

From (Hbufa), (Hbufb) and Definition 21, we only need to show:

$$\ll \mathbf{store} (a:L) (v:s) \rrbracket_L = \ll \mathbf{store} (a':L) (v':s') \rrbracket_L$$

which amounts to showing:

$$\ll (a:L) \rrbracket_L = \ll (a':L) \rrbracket_L \text{ and } \ll (v:s) \rrbracket_L = \ll (v':s') \rrbracket_L$$

With the same reasoning used in case EXECUTE-LOAD-COMMIT to prove (Ha), we can show that  $a = a'$ . Finally, from (Hapl), we have  $\ll (v:s) \rrbracket_L = \ll (v':s') \rrbracket_L$ , which by Lemma 9 entails  $\ll (v:s) \rrbracket_L = \ll (v':s') \rrbracket_L$ .

(Gtrans) The proof is similar to the proof for the case EXECUTE-ASSIGN.

This concludes the proof for the execute  $i$  directive.

**Retire.** For the retire directive, we have to consider the rules RETIRE-ASSIGN, RETIRE-STORE-LOW, and RETIRE-STORE-HIGH. In all RETIRE rules, the first instruction  $inst$  is removed from the reorder buffer:

$$buf_{n-1} = inst @ \varepsilon \cdot buf_n \text{ and } buf'_{n-1} = inst' @ \varepsilon \cdot buf'_n$$

Therefore, (Gbuf) follows from (IHbuf) and Definition 21. Additionally, we have:

$$\ll inst \rrbracket_L = \ll inst' \rrbracket_L \tag{Hinst}$$

From (IHstep), the first configuration can make a step. We first consider the case where the rule RETIRE-ASSIGN is applied; and then the case where the rules RETIRE-STORE-LOW or RETIRE-STORE-HIGH are applied.

RETIRE-ASSIGN: From the hypotheses of the rules, we have  $inst = r \leftarrow (v:s)$ , meaning that  $\ll inst \rrbracket_L = r \leftarrow \ll (v:s) \rrbracket_L$ . Therefore, from (Hinst), we have  $\ll inst' \rrbracket_L = r \leftarrow \ll (v:s) \rrbracket_L$  meaning that  $inst' = r \leftarrow (v':s')$ . Consequently, in the second configuration, the only rule that can be applied is RETIRE-ASSIGN.

Additionally, we have  $\ll (v:s) \rrbracket_L = \ll (v':s') \rrbracket_L$ , which by Lemma 9 gives us  $\ll (v:s) \rrbracket_L = \ll (v':s') \rrbracket_L$ .

In RETIRE-ASSIGN, the memory and the microarchitectural contexts are not modified. Therefore, (Gmem) (resp. (Gmicro)) directly follows from (IHmem) (resp. (IHmicro)). As we have already shown (Gbuf), it remains to show (Gstep) and (Greg).

(Gstep) We have shown that  $buf'_{n-1} = r \leftarrow \ll (v:s) \rrbracket_L \cdot buf'_n$ , hence the rule RETIRE-ASSIGN can also be applied in the second configuration, which entails (Gstep).

(Greg) The register maps are updated such that  $r_n \triangleq r_{n-1}[x \mapsto (v:s)]$  and  $r'_n \triangleq r'_{n-1}[x \mapsto (v':s')]$ . Therefore, (Greg), follows from  $(v:s)|_L = (v':s')|_L$  and (IHreg).

(Gtrans) Notice that  $buf_n = buf_{n-1}[2..|buf_{n-1}|]$  and  $buf'_n = buf'_{n-1}[2..|buf'_{n-1}|]$ . Additionally, we have  $r_n \triangleq r_{n-1}[x \mapsto (v:s)]$  and  $r'_n \triangleq r'_{n-1}[x \mapsto (v':s')]$ , as well as  $m_{n-1} = m_n$  and  $m'_{n-1} = m'_n$ . Hence, to show (Gtrans), we need to show:

$$\mathit{transient}(\langle m_n, r_{n-1}[x \mapsto (v:s)], buf_{n-1}[2..|buf_{n-1}|] \rangle) \iff \mathit{transient}(\langle m'_n, r'_{n-1}[x \mapsto (v':s')], buf'_{n-1}[2..|buf'_{n-1}|] \rangle)$$

This simply follows from (IHtrans), Definition 15 and Definition 17.

RETIRE-STORE-LOW or RETIRE-STORE-HIGH: From the hypotheses of the rules, we have  $inst = \mathbf{store} (a:s_a) (v:s_v)$ , meaning that  $\llbracket inst \rrbracket_L = \mathbf{store} \llbracket (a:s_a) \rrbracket_L \llbracket (v:s_v) \rrbracket_L$ . Therefore, from (Hinst), we have  $\llbracket inst' \rrbracket_L = \mathbf{store} \llbracket (a:s_a) \rrbracket_L \llbracket (v:s_v) \rrbracket_L$  meaning that  $inst' = \mathbf{store} (a':s'_a) (v':s'_v)$ . Consequently the only rules that can be applied in the second configuration are RETIRE-STORE-LOW and RETIRE-STORE-HIGH.

Additionally, we have:  $\llbracket (a:s_a) \rrbracket_L = \llbracket (a':s'_a) \rrbracket_L$  and  $\llbracket (v:s_v) \rrbracket_L = \llbracket (v':s'_v) \rrbracket_L$ , which from Lemma 9 entails  $\llbracket (a:s_a) \rrbracket_L = \llbracket (a':s'_a) \rrbracket_L$  and  $\llbracket (v:s_v) \rrbracket_L = \llbracket (v':s'_v) \rrbracket_L$ . Finally, because  $buf_n$  and  $buf_{n-1}$  are well-formed (cf. Lemma 2) and because store addresses have security level L in well-formed buffers (by Definition 16), we have  $s_a = s'_a = L$ . From  $\llbracket (a:s_a) \rrbracket_L = \llbracket (a':s'_a) \rrbracket_L$  this entails

$$a = a' \quad (\text{Ha})$$

In both rules, the register map is not modified. Therefore, (GREG) directly follows from (IHREG). As we have already shown (Gbuf), it remains to show (Gstep), (Gmem), (Gmicro) and (Gtrans).

(Gstep) We have shown that  $buf_{n-1}' = \mathbf{store} (a':s'_a) (v':s'_v) \cdot buf_n'$ , hence the rule RETIRE-STORE-LOW or the rule RETIRE-STORE-HIGH can also be applied in the second configuration, which entails (Gstep).

(Gmicro) In both rules, the microarchitectural context is modified such that  $\mu_n = \text{update}(\mu_{n-1}, a)$  and  $\mu'_n = \text{update}(\mu'_{n-1}, a')$ . Because  $\text{update}$  is deterministic (cf. Hyp. 1), (Gmicro) directly follows from (IHmicro) and (Ha).

(Gmem) In both rules, the memories are updated such that  $m_n \triangleq m_{n-1}[a \mapsto v]$  and  $m'_n \triangleq m'_{n-1}[a' \mapsto v']$ . Notice that from  $\llbracket (v:s_v) \rrbracket_L = \llbracket (v':s'_v) \rrbracket_L$  and Definition 20, we have  $s_v = s'_v$ . Hence, because we also have  $s_m(a) = s_m(a')$  from (Ha), both executions evaluate the same rule. We first consider the case in which both executions evaluate the rule RETIRE-STORE-LOW and then, the case where both executions evaluate the rule RETIRE-STORE-HIGH:

- In case RETIRE-STORE-LOW, we need to show  $v = v'$ . By (IHarch), we get that  $\langle m_{n-1}, r_{n-1} \rangle = \alpha_j$  and  $\langle m'_{n-1}, r'_{n-1} \rangle = \alpha'_j$  where  $j = \text{corr}_{\vec{\alpha}, \vec{c}}(n-1)(0)$ . From Definition 16, we know that  $P[\llbracket \text{PC} \rrbracket_{r_{n-1}}] = P[\llbracket \text{PC} \rrbracket_{r'_{n-1}}] = \mathbf{store} e_a e_v$ . Additionally, we have  $v = \llbracket e_v \rrbracket_r$  and  $v' = \llbracket e_v \rrbracket_{r'}$  and  $a = \llbracket e_a \rrbracket_r = \llbracket e_a \rrbracket_{r'}$ . Consequently, we can apply the STORE rule in the sequential semantics (Fig. 8) to  $\alpha_j$  and  $\alpha'_j$ . Additionally, from  $a = \llbracket e_a \rrbracket_r = \llbracket e_a \rrbracket_{r'}$  and  $s_m(a) = L$ , we know that the evaluation of the rule in both configurations produce non-empty declassification traces  $\mathbf{v}$  and  $\mathbf{v}'$ . Moreover, from Hyp. 2, we have  $\mathbf{v} = \mathbf{v}'$ . Finally, by the rule RETIRE-STORE-LOW we have  $m_n \triangleq m_{n-1}[a \mapsto v]$  and  $m'_n \triangleq m'_{n-1}[a \mapsto v]$ . Therefore (Gmem) follows from (IHmem).
- In case RETIRE-STORE-HIGH, we have  $s_m(a) = H$  so the public memory is not modified, meaning that (Gmem) follows from (IHmem) and Definition 3.

(Gtrans) The proof is similar to the case RETIRE-ASSIGN.

This concludes the proof for the retire directive, and in turn, for Lemma 16.  $\square$

**Theorem 1** (Security for constant-time programs.). *For any constant-time program that does not declassify secret data, microarchitectural state  $\mu_0$ , initial configurations  $c_0 = \langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and  $c'_0 = \langle m'_0, r'_0, \varepsilon, \mu_0 \rangle$  such that  $\langle m_0, r_0 \rangle_L = \langle m'_0, r'_0 \rangle_L$  and number of steps  $n$ ,*

$$c_0 \rightarrow^n c_n \implies c'_0 \rightarrow^n c'_n \wedge \mu_n = \mu'_n$$

where  $\mu_n$  and  $\mu'_n$  are the microarchitectural contexts in configurations  $c_n$  and  $c'_n$ , respectively.

*Proof.* Proof follows from the direct application of Lemma 16.  $\square$

## E.4 Correspondence between patched architectural and patched hardware semantics

**Notations** Through this section, we call a (architectural or hardware) configuration  $c$  with a declassification trace  $\delta$ , denoted  $(c, \delta)$ , a *patched configuration*. We let  $\vec{\alpha}_\delta$  (resp.  $\vec{c}_\delta$ ) denote a sequence of patched architectural configuration or (resp. patched hardware configuration) resulting from a execution in the architectural (resp. hardware) semantics patched with  $\delta$ . Given a sequence of patched architectural configurations  $\vec{\alpha}_\delta$ , we let  $(\alpha_j, \delta_j)$  with  $0 \leq j \leq |\vec{\alpha}|$  denote the  $j^{\text{th}}$  configuration in  $\vec{\alpha}$  (the same holds for  $\vec{c}$ ).

The deep update of a patched architectural configuration  $(\langle m, r \rangle, \delta)$  and reorder buffer  $buf$ , denoted  $(\langle m, r \rangle, \delta) \uplus \varepsilon$ , applies all pending instructions in  $buf$  to the configuration  $(\langle m, r \rangle, \delta)$ . That the deep update for patched configurations is similar to the deep update defined in Definition 15 except that it replaces values stored to low-memory with values from the declassification trace.

**Definition 22** (Patched deep update). For any reorder buffer  $buf$  and patched architectural configuration  $\langle m, r \rangle, \delta$ :

$$\begin{aligned}
& \langle m, r \rangle, \delta \uplus \varepsilon \triangleq \langle m, r \rangle, \delta \\
& \langle m, r \rangle, \delta \uplus x \leftarrow e @ T \triangleq \begin{cases} \langle m, r[x \mapsto \llbracket e \rrbracket_r] \rangle, \delta & \text{if } T = \varepsilon \\ \langle m, r[x \mapsto m(\llbracket e_a \rrbracket_r)] \rangle, \delta & \text{if } T = 1 \wedge P[1] = x \leftarrow \mathbf{load } e_a \end{cases} \\
& \langle m, r \rangle, \delta \uplus pc \leftarrow e @ T \triangleq \begin{cases} \langle m, r[pc \mapsto \llbracket e \rrbracket_r] \rangle, \delta & \text{if } T = \varepsilon \\ \langle m, r[pc \mapsto \llbracket e_l \rrbracket_r] \rangle, \delta & \text{if } T = 1 \wedge P[1] = \mathbf{jmp } e_l \\ \langle m, r[pc \mapsto 1'] \rangle, \delta & \text{if } T = 1 \wedge P[1] = \mathbf{beqz } e_c \ 1' \wedge \llbracket e_c \rrbracket_r = 0 \\ \langle m, r[pc \mapsto 1 + 1] \rangle, \delta & \text{if } T = 1 \wedge P[1] = \mathbf{beqz } e_c \ 1' \wedge \llbracket e_c \rrbracket_r \neq 0 \end{cases} \\
& \langle m, r \rangle, \delta \uplus x \leftarrow \mathbf{load } e_a @ T \triangleq \langle m, r[x \mapsto m(\llbracket e_a \rrbracket_r)] \rangle, \delta \\
& \langle m, r \rangle, \delta \uplus \mathbf{store } e_a \ e_v @ T \triangleq \begin{cases} \langle m[a \mapsto v], r \rangle, \delta' & \text{if } a \triangleq \llbracket e_a \rrbracket_r \wedge s_m(a) = L \wedge \delta = v \cdot \delta' \\ \langle m[a \mapsto \llbracket e_v \rrbracket_r], r \rangle, \delta & \text{if } a \triangleq \llbracket e_a \rrbracket_r \wedge s_m(a) = H \end{cases} \\
& \langle m, r \rangle, \delta \uplus (inst @ T \cdot buf) \triangleq (\langle m, r \rangle, \delta) \uplus inst @ T \uplus buf
\end{aligned}$$

The well-formed buffer predicate for patched configurations,  $wf(buf, \langle m, r \rangle, \delta)$ , can be obtained from Definition 16 by replacing the deep projection with the patched deep projection;  $transient(\langle c, \delta \rangle)$ ,  $goodpred(inst @ \varepsilon, \langle m, r \rangle, \delta)$   $prefix(buf, \langle m, r \rangle, \delta)$ , and  $corr_{\vec{\alpha}_\delta, \vec{c}_\delta}$  can be obtained similarly.

The following lemma states that for all non-transient buffer  $buf$  with respect to a configuration  $\langle m, r \rangle$ , the register map obtained by the function  $apl$  is equivalent (when defined) to the register map obtained by the deep update of  $buf$  with  $\langle m, r \rangle$ .

**Lemma 17.** *Let  $\langle m, r \rangle, \delta$  be an architectural configuration and  $buf$  a reorder buffer such that  $\neg transient(\langle m, r, buf, \_ \rangle)$ . Let  $(\_, r'), \_ = \langle m, r \rangle, \delta \uplus buf$ . We have that for all  $\tau$  if  $apl(buf, r)(\tau) = (v:s)$  then  $r'(\tau) = (v:s)$ .*

*Proof.* The proof is similar to the proof for Lemma 4. In particular, it goes by induction on the size of the ROB, Definition 2 and Definition 22. The only case that differ is the case  $inst = \mathbf{store } e_a \ e_v @ T$ . Notice that the instruction is ignored by  $apl$  but the memory is modified (and possibly patched using the declassification trace) in  $\uplus$ . However, it may only impacts the result of subsequent  $inst = x \leftarrow \mathbf{load } e @ T$  instructions but these instructions result in undefined  $x$  with  $apl$ , which immediately concludes our goal.  $\square$

It follows that Corollaries 2 and 3 can also be applied to patched configurations.

The following lemma states that for each patched hardware state in a patched hardware run, for all the prefixes of its reorder buffer, there exists a corresponding patched architectural state in the corresponding patched architectural run.

**Lemma 18** (Correctness of the  $corr_{\vec{\alpha}_\delta, \vec{c}_\delta}$  relation). *Let  $\alpha_0 = \langle m, r \rangle$  be an initial architectural configuration,  $\mu$  be a microarchitectural context and  $\delta$  a declassification trace. Additionally, let  $\vec{\alpha}_\delta$  be the longest contract run, starting from  $(\alpha_0, \delta)$ , and  $\vec{c}_\delta$  be the longest PROSPECT run starting from  $(\langle m, r, \varepsilon, \mu \rangle, \delta)$ . Additionally, for all  $0 \leq n < |\vec{c}|$ , we let  $(c_n, \delta_n)$  denote the  $n^{\text{th}}$  configuration in  $\vec{c}$ , and for all  $0 \leq j < |\vec{\alpha}|$ , we let  $\vec{\alpha}[j]$  be the  $j^{\text{th}}$  architectural configuration in  $\vec{\alpha}$ .*

*For all  $0 \leq n < |\vec{c}|$ , we have:*

$$\text{For all } buf \in prefix(buf_n, (\langle m_n, r_n \rangle, \delta_n)), (\langle m_n, r_n \rangle, \delta_n) \uplus buf = \vec{\alpha}[j] \text{ where } j = corr_{\vec{\alpha}_\delta, \vec{c}_\delta}(n)(|buf|). \quad (\text{G})$$

*Proof.* The proof goes by induction on  $n$ .

**Base case** ( $n = 0$ ). We have  $c_0 = (\langle m, r, \varepsilon, \mu \rangle, \delta)$ , hence  $buf_0 = \varepsilon$ . From Definition 18, we have that  $prefix(\varepsilon) = \{\varepsilon\}$ . Additionally, from Definition 19, we have that  $j = corr_{\vec{\alpha}_\delta, \vec{c}_\delta}(0)(|\varepsilon|) = 0$ . From Definition 15, we have that  $(\langle m, r \rangle, \delta) \uplus \varepsilon = (\langle m, r \rangle, \delta) = \vec{\alpha}[0]$ , which concludes (G).

**Inductive case.** Assume that the hypothesis holds for hardware runs of length  $n - 1$ , namely:

$$\text{For all } buf \in prefix(buf_{n-1}, (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1})), (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}) \uplus buf = \vec{\alpha}[j] \text{ where } j = corr_{\vec{\alpha}_\delta, \vec{c}_\delta}(n-1)(|buf|). \quad (\text{IH})$$

We show that (G) holds at step  $n$ . The proof is similar to the proof for Lemma 5 except for the rules FETCH-OTHERS, EXECUTE-STORE and RETIRE-STORE.

FETCH-OTHERS: from the evaluation rules (cf. Fig. 4), we have  $buf_n = buf_{n-1} \cdot inst @ \varepsilon \cdot pc \leftarrow (1 + 1:L) @ \varepsilon$  where  $(1:_) \triangleq \llbracket pc \rrbracket_{apl}(buf_{n-1}, r_{n-1})$ ,  $inst = P[1]$  and  $inst \notin \{ \mathbf{beqz} \_ \_, \mathbf{jmp} \_ \_ \}$ . Additionally, we have  $m_n = m_{n-1}$ ,  $r_n = r_{n-1}$  and  $\delta_n = \delta_{n-1}$ . As in the proof for Lemma 5, there are several cases to consider. We focus here on the case  $\neg transient(c_{n-1})$ , which means  $prefix(buf_n, (\langle m_n, r_n \rangle, \delta_n)) = prefix(buf_{n-1}, (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1})) \cup \{buf_n\}$ ; and in particular the case  $buf \in prefix(buf_n, (\langle m_n, r_n \rangle, \delta_n)) = buf_n = buf_{n-1} \cdot inst @ \varepsilon \cdot pc \leftarrow (1 + 1:L) @ \varepsilon$  with  $inst = \mathbf{store} e_a e_v$ . The other cases are similar to the proof for Lemma 5. In particular, when we need to show that the sequential semantics and the patched deep update would produce the same changes on a configuration, we can observe that the declassification trace is simply propagated by the sequential semantics and by the patched deep update Definition 22 and not modified.

In that case, because  $\neg transient(c_{n-1})$  and because reorder buffers are well-formed (Lemma 2), we have from Definition 18 that  $buf_{n-1} \in prefix(buf_{n-1}, (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}))$ . Hence, from (IH), we have

$$(\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}) \uplus buf_{n-1} = \bar{\alpha}[j] \text{ where } j = corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)(|buf_{n-1}|)$$

In the following, we let  $\bar{\alpha}[j] = (\langle r_j, m_j \rangle, \delta_j)$ . From Corollary 2 and  $(1:_) = \llbracket pc \rrbracket_{apl}(buf_{n-1}, r_{n-1})$ , we have  $r_j(pc) = (1:_)$  and hence  $lst\_pc((c_{n-1}, \delta_{n-1})) = 1$ , meaning that  $P[lst\_pc(c_{n-1})] = \mathbf{store} e_a e_v$ . From this, Definition 19, and  $|buf| = |buf_{n-1}| + 2$ , we get  $corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n)(|buf|) = corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)(|buf_{n-1}|) + 1 = j + 1$ .

Additionally, from Definition 22, we have that

$$(\langle m_n, r_n \rangle, \delta_n) \uplus buf = (((\langle m_n, r_n \rangle, \delta_n) \uplus buf_{n-1}) \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon$$

From  $(\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}) = (\langle m_n, r_n \rangle, \delta_n)$ , and the definition of  $\bar{\alpha}[j]$ , this gives us  $(\langle m_n, r_n \rangle, \delta_n) \uplus buf = (\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon$ . Hence, in order to show  $(\langle m_n, r_n \rangle, \delta_n) \uplus buf = \bar{\alpha}[corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n)(|buf|)]$  (which concludes our goal (G) for this case), it remains to show

$$(\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \bar{\alpha}[j + 1]$$

Let  $a = \llbracket e_a \rrbracket_{r_j}$ . Next, we consider the case where  $a$  corresponds to public memory and the case where  $a$  corresponds to secret memory.

- In case  $s_m(a) = H$ , from Definition 22, we have  $(\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = (\langle m_j[a \mapsto \llbracket e_v \rrbracket_{r_j}], r_j[pc \mapsto 1 + 1] \rangle, \delta_j)$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 9, rule STORE-HIGH), we also have  $\bar{\alpha}[j + 1] = (\langle m_j[a \mapsto \llbracket e_v \rrbracket_{r_j}], r_j[pc \mapsto 1 + 1] \rangle, \delta_j)$ , which concludes  $(\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \bar{\alpha}[j + 1]$ .
- In case  $s_m(a) = L$ , from Definition 22, we have  $(\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = (\langle m_j[a \mapsto v], r_j[pc \mapsto 1 + 1] \rangle, \delta')$  where  $\delta_j = v \cdot \delta'$ . Moreover, from the evaluation rules of the sequential semantics (Fig. 9, rule STORE-PATCHED), we also have  $\bar{\alpha}[j + 1] = (\langle m_j[a \mapsto v], r_j[pc \mapsto 1 + 1] \rangle, \delta')$ , which concludes  $(\bar{\alpha}[j] \uplus \mathbf{store} e_a e_v @ \varepsilon) \uplus pc \leftarrow (1 + 1:L) @ \varepsilon = \bar{\alpha}[j + 1]$ .

EXECUTE-STORE: In this case, the directive that is applied is  $d = \mathbf{execute} j$  and from Definition 19, we have  $corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n) = corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)$ . Additionally, from the hardware evaluation rules (cf. Fig. 6), we have  $(\langle m_n, r_n \rangle, \delta_n) = (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1})$ , and:

$$\begin{aligned} buf_{n-1} &= buf_{n-1}[1..j-1] \cdot \mathbf{store} e_a e_v @ T \cdot buf_{n-1}[j+1..|buf_{n-1}|] \\ buf_n &= buf_{n-1}[1..j-1] \cdot \mathbf{store} (a:L) (v:_ ) @ T \cdot buf_{n-1}[j+1..|buf_{n-1}|] \end{aligned}$$

with  $e_a \notin \hat{\mathcal{V}}$ ,  $e_v \notin \hat{\mathcal{V}}$ ,  $(a:_ ) = \llbracket e_a \rrbracket_{apl}(buf_{n-1}[1..j-1], r_{n-1})$ , and  $(v:_ ) = \llbracket e_v \rrbracket_{apl}(buf_{n-1}[1..j-1], r_{n-1})$ .

Let  $buf$  be an arbitrary prefix in  $prefix(buf_n, (\langle m_n, r_n \rangle, \delta_n))$ . We can consider two cases:

- $|buf| < j$ . The proof for this case is similar to the proof for the corresponding case in Lemma 5.
- $|buf| \geq j$ . Notice that, by Definition 18 and  $buf \in prefix(buf_n, (\langle m_n, r_n \rangle, \delta_n))$ , there is no misspredicted instruction in  $buf$  (except possibly the last one). Therefore, it follows from  $(\langle m_n, r_n \rangle, \delta_n) = (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1})$ , that  $buf' = buf[1..j-1] \cdot \mathbf{store} e_a e_v @ T \cdot buf[j+1..|buf|]$  belongs to  $prefix(buf_{n-1}, (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}))$ . Hence, from (IH), we have that

$$(\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1}) \uplus buf' = \bar{\alpha}[corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)(|buf'|)]$$

From this,  $|buf'| = |buf|$ ,  $(\langle m_n, r_n \rangle, \delta_n) = (\langle m_{n-1}, r_{n-1} \rangle, \delta_{n-1})$ , and  $corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n) = corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)$ , we get that

$$(\langle m_n, r_n \rangle, \delta_n) \uplus buf' = \bar{\alpha}[corr_{\bar{\alpha}_\delta, \bar{c}_\delta}(n)(|buf|)]$$

Let  $(\langle m', r' \rangle, \delta') = (\langle m_n, r_n \rangle, \delta_n) \uplus buf_{n-1}[1..j-1]$ . Notice that from Lemma 17,  $r_n = r_{n-1}$ ,  $(a:_ ) = \llbracket e_a \rrbracket_{apl}(buf_{n-1}[1..j-1], r_{n-1})$ , and  $(v:_ ) = \llbracket e_v \rrbracket_{apl}(buf_{n-1}[1..j-1], r_{n-1})$ , we get  $(a:_ ) = \llbracket e_a \rrbracket_{r'}$  and  $(v:_ ) = \llbracket e_v \rrbracket_{r'}$ . From there, we consider two cases:

–  $s_m(a) = L$ . In this case, by Definition 22 and rewriting we get

$$\begin{aligned} \langle (m_n, r_n), \delta_n \rangle \uplus buf' &= \langle (m', r'), \delta' \rangle \uplus \mathbf{store} \ e_a \ e_v @ T \cdot buf[j+1..|buf|] \\ &= \langle (m'[a \mapsto v'], r'), \delta'' \rangle \uplus buf[j+1..|buf|] \text{ where } \delta' = v \cdot \delta'' \\ &= \langle (m', r'), \delta' \rangle \uplus \mathbf{store} \ (a:\_) \ (v:\_) @ T \cdot buf[j+1..|buf|] \\ &= \langle (m_n, r_n), \delta_n \rangle \uplus buf \end{aligned}$$

which means  $\langle (m_n, r_n), \delta_n \rangle \uplus buf = \bar{\alpha}[\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n)(|buf|)]$  and concludes (G).

–  $s_m(a) = H$ . In this case, by Definition 22 and rewriting we get

$$\begin{aligned} \langle (m_n, r_n), \delta_n \rangle \uplus buf' &= \langle (m', r'), \delta' \rangle \uplus \mathbf{store} \ e_a \ e_v @ T \cdot buf[j+1..|buf|] \\ &= \langle (m'[a \mapsto v], r'), \delta' \rangle \uplus buf[j+1..|buf|] \\ &= \langle (m', r'), \delta' \rangle \uplus \mathbf{store} \ (a:\_) \ (v:\_) @ T \cdot buf[j+1..|buf|] \\ &= \langle (m_n, r_n), \delta_n \rangle \uplus buf \end{aligned}$$

which concludes (G).

RETIRE-STORE-LOW and RETIRE-STORE-HIGH. In this case, from Definition 19, we have  $\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n) = \text{shift}(\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1))$ . Moreover, from the hardware evaluation rules in Fig. 7, we have  $buf_{n-1} = \mathbf{store} \ (a:\_) \ (v:\_) @ \varepsilon \cdot buf_n$ . From here, we consider the cases  $s_m(a) = L$  and  $s_m(a) = H$  separately. We only detail the case  $s_m(a) = L$  as the proof for the other case is similar to the corresponding proof case in the proof of Lemma 5.

In the case  $s_m(a) = L$ , the rule RETIRE-STORE-LOW is applied and we have  $\delta_{n-1} = v' \cdot \delta_n$ ,  $m_n = m_{n-1}[a \mapsto v']$ , and  $r_n = r_{n-1}$ . Additionally, because  $buf_{n-1}$  is well-formed (cf. Lemma 2) and from the definition of well-formed buffers (Definition 16), we have that  $buf_n = \text{pc} \leftarrow^* (1:L) \cdot buf'_{n-1}$ . Hence, from Definition 18, we have

$$\begin{aligned} \text{prefix}(buf_{n-1}, \langle (m_{n-1}, r_{n-1}), \delta_{n-1} \rangle) &= \{\varepsilon\} \cup \{ \mathbf{store} \ (a:\_) \ (v:\_) @ \varepsilon \cdot \text{pc} \leftarrow (1:L) @ \varepsilon \cdot buf' \mid \\ &\quad buf' \in \text{prefix}(buf'_{n-1}, \langle (m_{n-1}, r_{n-1}), \delta_{n-1} \rangle) \uplus \mathbf{store} \ (a:\_) \ (v:\_) @ \varepsilon \cdot \text{pc} \leftarrow (1:L) @ \varepsilon \} \\ \text{prefix}(buf_n, \langle (m_n, r_n), \delta_n \rangle) &= \{\varepsilon\} \cup \{ \text{pc} \leftarrow (1:L) @ \varepsilon \cdot buf' \mid buf' \in \text{prefix}(buf'_{n-1}, \langle (m_{n-1}, r_{n-1}), \delta_{n-1} \rangle) \uplus \text{pc} \leftarrow (1:L) @ \varepsilon \} \end{aligned}$$

Let  $buf$  be an arbitrary prefix in  $buf_n$ . By Definition 18 and the definition of  $buf_n$  and  $buf_{n-1}$ , we have that  $\mathbf{store} \ (a:\_) \ (v:\_) @ \varepsilon \cdot buf$  is a prefix in  $\text{prefix}(buf_{n-1}, \langle (m_{n-1}, r_{n-1}), \delta_{n-1} \rangle)$ . Hence, from (IH), we have

$$\langle (m_{n-1}, r_{n-1}), \delta_{n-1} \rangle \uplus \mathbf{store} \ (a:\_) \ (v:\_) @ \varepsilon \cdot buf = \bar{\alpha}[j] \text{ where } j = \text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)(|buf| + 1)$$

Hence, by  $\delta_{n-1} = v' \cdot \delta_n$  and Definition 22, we get  $\langle (m_{n-1}[a \mapsto v'], r_{n-1}), \delta_n \rangle \uplus buf = \bar{\alpha}[j]$ . By  $m_n = m_{n-1}[a \mapsto v']$  and  $r_n = r_{n-1}$ , this gives us  $\langle (m_n, r_n), \delta_n \rangle \uplus buf = \bar{\alpha}[j]$ . Finally, by definition of *shift*, we get

$$\langle (m_n, r_n), \delta_n \rangle \uplus buf = \bar{\alpha}[\text{shift}(\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1)(|buf|))]$$

which from  $\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n) = \text{shift}(\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n-1))$ , entails  $\langle (m_n, r_n), \delta_n \rangle \uplus buf = \bar{\alpha}[\text{corr}_{\bar{\alpha}_\delta, \bar{c}_\delta}(n)(|buf|)]$  and concludes (G).

We have shown for any evaluation rule in the hardware semantics that if (G) holds at step  $n-1$ , then it also holds at step  $i$ . This concludes the proof of Lemma 18.  $\square$

## E.5 Proof of security for constant-time programs with declassification

The following hypotheses are used to prove security for constant-time programs with declassification:

**Hypothesis 1.** The functions *predict*, *update*, and *next* are deterministic.

**Hypothesis 3.** The program is constant-time up to declassification (according to Definition 7). In particular, it means that for all configurations  $\langle r_0, m_0 \rangle$  and  $\langle r'_0, m'_0 \rangle$  such that  $r_0|_L = r'_0|_L$  and  $m_0|_L = m'_0|_L$ , and for all number of step  $n$ ,

$$\langle m_0, r_0 \rangle \xrightarrow{\delta}_o^n \langle m_n, r_n \rangle \implies \langle (m'_0, r'_0), \delta \rangle \xrightarrow{o'}^n \langle (m'_n, r'_n), \varepsilon \rangle \wedge o = o'$$



Additionally, the following contract emphasizes that software-developer should make sure to not unintentionally declassify secrets by writing them to public locations.

**Contract 3.** Secret values written to public memory are *intentionally declassified* by the program.

The following lemma expresses that given a n-step patched execution, which from an initial declassification trace  $\delta_i$  produces a declassification trace  $\delta_f$ , adding a suffix  $\delta$  to the declassification trace does not change the execution and the final declassification trace becomes  $\delta_f \cdot \delta$ :

**Lemma 19.** For all configuration  $\langle m'_0, r'_0, buf_0, \mu_0 \rangle$ , number of steps  $n$  and declassification traces  $\delta_i$ ,  $\delta_f$ , and  $\delta$ :

$$\begin{aligned} \langle m_0, r_0, buf_0, \mu_0 \rangle, \delta_i &\hookrightarrow^n \langle m_n, r_n, buf_n, \mu_n \rangle, \delta_f \implies \\ \langle m_0, r_0, buf_0, \mu_0 \rangle, \delta_i \cdot \delta &\hookrightarrow^n \langle m_n, r_n, buf_n, \mu_n \rangle, \delta_f \cdot \delta \end{aligned}$$

*Proof.* The proof goes by induction on the number of steps. The base case directly follows from Definition 11: for a 0-step execution, the declassification trace is simply forwarded:  $(c, \delta_i) \hookrightarrow^0 (c, \delta_i)$ . Therefore, adding a suffix to the declassification trace does not change the execution and declassification trace is forwarded with its suffix:  $(c, \delta_i \cdot \delta_d) \hookrightarrow^0 (c, \delta \cdot \delta_d)$ .

We assume that the hypothesis holds for  $n - 1$  steps and show that it still holds after  $n$  steps. From Definition 11, this amounts to showing:

$$\begin{aligned} \langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle, \delta_i &\hookrightarrow \langle m_n, r_n, buf_n, \mu_n \rangle, \delta_f \implies \\ \langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle, \delta_i \cdot \delta &\hookrightarrow \langle m_n, r_n, buf_n, \mu_n \rangle, \delta_f \cdot \delta \end{aligned} \quad (\text{G})$$

The proof proceeds by case analysis on the hardware evaluation. Notice that all the rules except RETIRE-STORE-PATCHED do not use the declassification trace and simply forward it to the next configuration (i.e.,  $\delta_i = \delta_f$ ). Therefore, for these rules, adding a suffix  $\delta$  to the declassification trace  $\delta_i$  does not change the execution: the same rule is applied and the same configuration is returned because the semantics is deterministic (cf. Hyp. 1). Moreover, the declassification trace with its suffix  $\delta_i \cdot \delta$  is forwarded to the next configuration, which concludes (G).

For the rule RETIRE-STORE-PATCHED, we have  $\delta_i = v \cdot \delta_f$ . In this case, the application of the rule with  $\delta_i \cdot \delta$  does not change the execution (the same microarchitectural configuration is returned) and produces a final declassification trace  $\delta_f \cdot \delta$ , which conclude (G).  $\square$

The following lemma expresses that the hardware semantics and the architectural semantics produce the same declassification traces:

**Lemma 20.** For all initial architectural configuration  $\langle r, m \rangle$  and microarchitectural context  $\mu$ , let  $\vec{\alpha}$  be the longest architectural run starting from  $\langle r, m \rangle$  and producing a declassification trace  $\delta$ ; and  $\vec{c}$  be the longest PROSPECT run starting from  $c_0 = \langle m, r, \varepsilon, \mu \rangle$  and producing a declassification trace  $\delta'$ . Then we have  $\delta = \delta'$ .

*Proof.* The proof goes by induction on the hardware evaluation.

First, note that the sequence of retired instructions (excluding  $\text{pc} \stackrel{*}{\leftarrow} \_$ ) corresponds to the sequence of architectural instructions (by Definition 19). Hence, for the  $i^{\text{th}}$  instruction that is retired in the hardware semantics (excluding  $\text{pc} \stackrel{*}{\leftarrow} \_$ ) and corresponding to configuration  $n$ , we have that  $\text{corr}_{\vec{\alpha}, \vec{c}}(n)(0) = i$ . Second, note that the only rule in the hardware semantics that produces a declassification trace is RETIRE-STORE-LOW.

Hence it suffices to show that the sequence of retired instructions produces the same declassification events  $\delta_i$  than the architectural semantics.

Let us consider the  $i^{\text{th}}$  instruction that is retired in the hardware semantics (excluding  $\text{pc} \stackrel{*}{\leftarrow} \_$ ) and corresponding to configuration  $n$ . We show that the corresponding architectural configuration  $\alpha_i$  produces the same declassification trace.

If the retired instruction is retired using RETIRE-STORE-LOW (cf. Fig. 7), then the retired instruction is a **store**, it writes a value  $v$  at an address  $a$  such that  $s_m(a) = L$  and it produces a declassification trace  $valv$  that is the value written to memory by the store. From Lemma 5 (and because  $\varepsilon$  is a prefix of  $buf_n$ ), we have that the corresponding state  $\alpha_i$  (cf. Fig. 8) also evaluates the rule STORE with index  $a$  and value  $v$ . Hence it also produces a declassification trace  $valv$ .

If the retired instruction is retired using RETIRE-STORE-HIGH or RETIRE-ASSIGN, we can show in a similar way that the declassification trace will be empty in the hardware and in the architectural semantics.

We have show that declassification events only happen when retiring instructions, that the sequence of retired instructions corresponds to  $\vec{\alpha}$ , and that retired instructions produce the same declassification events as their corresponding architectural step. Hence the declassification traces produced by  $\vec{\alpha}$  and  $\vec{c}$  are equal.  $\square$

This is the main lemma:

**Lemma 21.** *Assuming Hyp. 1, for all program  $P$  satisfying Hyp. 3 (and assuming Contract 3), for all number of steps  $n$ , memories  $m_0$  and  $m'_0$ , register maps  $r_0$  and  $r'_0$ , and microarchitectural context  $\mu_0$ ,*

$$\begin{aligned}
m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \wedge r'_0|_{\mathbb{L}} = r_0|_{\mathbb{L}} \wedge \langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta_{0:n}}^n \langle m_n, r_n, buf_n, \mu_n \rangle &\implies \\
(\langle m'_0, r'_0, \varepsilon, \mu_0 \rangle, \delta_{0:n}) \hookrightarrow^n (\langle m'_n, r'_n, buf'_n, \mu'_n \rangle, \varepsilon) \wedge &\quad (\text{Gstepn}) \\
\llbracket buf_n \rrbracket_{\mathbb{L}} = \llbracket buf'_n \rrbracket_{\mathbb{L}} \wedge &\quad (\text{Gbuf}) \\
\|r_n\|_{\mathbb{L}} = \|r'_n\|_{\mathbb{L}} \wedge &\quad (\text{Greg}) \\
m_n|_{\mathbb{L}} = m'_n|_{\mathbb{L}} \wedge &\quad (\text{Gmem}) \\
\mu_n = \mu'_n \wedge &\quad (\text{Gmicro}) \\
\text{corr}_{\vec{\alpha}, \vec{c}}(n) = \text{corr}_{\vec{\alpha}'_n, \vec{c}'_n}(n) \wedge &\quad (\text{Gcorr}) \\
\forall 0 \leq i \leq |buf_n|. \text{transient}(\langle m_n, r_n, buf_n[0..i], \_ \rangle) = \text{transient}(\langle m'_n, r'_n, buf'_n[0..i], \_ \rangle, \delta_n) &\quad (\text{Gtrans})
\end{aligned}$$

where  $\vec{\alpha}$  is the longest architectural run starting from  $\langle m_0, r_0 \rangle$ ,  $\vec{c}$  is the longest PROSPECT run starting from  $\langle m_0, r_0, \varepsilon, \mu \rangle$  and producing a declassification trace  $\delta$ ,  $\vec{\alpha}'_n$  is the longest patched architectural run starting from  $(\langle m'_0, r'_0 \rangle, \delta)$ ,  $\vec{c}'_n$  is the longest patched PROSPECT run starting from  $(\langle m'_0, r'_0, \varepsilon, \mu \rangle, \delta)$ , and  $\delta_n$  is the declassification trace of  $\vec{c}'_n[n]$ .

*Proof.* Assume a program  $P$  satisfying Hyp. 3, memories  $m_0$  and  $m'_0$ , register maps  $r_0$  and  $r'_0$ , and a microarchitectural context  $\mu_0$ , such that:

$$m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \text{ and } r_0|_{\mathbb{L}} = r'_0|_{\mathbb{L}} \quad (\text{Hloweq})$$

$$\langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta_{0:n}}^n \langle m_n, r_n, buf_n, \mu_n \rangle \quad (\text{Hstepn})$$

Under these hypothesis, we show that (Gstepn), (Gbuf), (Gmem), (Gmicro), (Gcorr), and (Gtrans). The proof goes by induction on the number of steps  $n$ .

**Base case ( $n = 0$ ):**

(Gstepn) From Definition 10, a 0-step execution from the first configuration produces a declassification trace  $\varepsilon: \langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\varepsilon}^0 \langle m_0, r_0, buf_0, \mu_0 \rangle$ . Hence, from Definition 11, in the second configuration, we have:  $(\langle m'_0, r'_0, buf'_0, \mu'_0 \rangle, \varepsilon) \hookrightarrow^0 (\langle m'_0, r'_0, buf'_0, \mu'_0 \rangle, \varepsilon)$

$$(\text{Gbuf}) \llbracket buf_0 \rrbracket_{\mathbb{L}} = \llbracket buf'_0 \rrbracket_{\mathbb{L}} = \varepsilon$$

$$(\text{Greg}) \|r_0\|_{\mathbb{L}} = \|r'_0\|_{\mathbb{L}} \text{ follows from the application of Corollary 4 with (Hloweq) and Lemma 3,}$$

$$(\text{Gmem}) m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \text{ directly follows from (Hloweq),}$$

$$(\text{Gmicro}) \mu_0 = \mu'_0 \text{ because the initial microarchitectural context is the same in both initial configurations,}$$

$$(\text{Gcorr}) \text{corr}_{\vec{\alpha}, \vec{c}}(0) = \text{corr}_{\vec{\alpha}'_0, \vec{c}'_0}(0) = \{0 \mapsto 0\} \text{ by Definition 19,}$$

(Gtrans)  $\forall 0 \leq i \leq |buf_0|. \text{transient}(\langle m_0, r_0, buf_0[0..i], \mu_0 \rangle) = \text{transient}(\langle m'_0, r'_0, buf'_0[0..i], \mu'_0 \rangle, \delta_0)$  follows directly by definition of *transient* (cf. Definition 17) and  $buf_0 = buf'_0 = \varepsilon$ .

**Inductive case:** We assume that Lemma 21 holds at step  $n - 1$ , meaning that:

$$\begin{aligned}
m_0|_{\mathbb{L}} = m'_0|_{\mathbb{L}} \wedge r'_0|_{\mathbb{L}} = r_0|_{\mathbb{L}} \wedge \langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta_{0:n-1}}^{n-1} \langle m_{n-1}, r_{n-1}, buf_{n-1}, \mu_{n-1} \rangle &\implies \\
(\langle m'_0, r'_0, \varepsilon, \mu_0 \rangle, \delta_{0:n-1}) \hookrightarrow^{n-1} (\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle, \varepsilon) &\quad (\text{IHstepn}) \\
\llbracket buf_{n-1} \rrbracket_{\mathbb{L}} = \llbracket buf'_{n-1} \rrbracket_{\mathbb{L}} &\quad (\text{IHbuf}) \\
\|r_{n-1}\|_{\mathbb{L}} = \|r'_{n-1}\|_{\mathbb{L}} &\quad (\text{IHreg}) \\
m_{n-1}|_{\mathbb{L}} = m'_{n-1}|_{\mathbb{L}} &\quad (\text{IHmem}) \\
\mu_{n-1} = \mu'_{n-1} &\quad (\text{IHmicro}) \\
\text{corr}_{\vec{\alpha}, \vec{c}}(n-1) = \text{corr}_{\vec{\alpha}'_{n-1}, \vec{c}'_{n-1}}(n-1) &\quad (\text{IHcorr})
\end{aligned}$$

$$\forall 0 \leq i \leq |buf_{n-1}|. \text{transient}(\langle m_{n-1}, r_{n-1}, buf_{n-1}[0..i], \_ \rangle) = \text{transient}(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}[0..i], \_ \rangle, \delta_{n-1}) \quad (\text{IHtrans})$$

Under these hypotheses, we show that Lemma 16 still holds at step  $n$ .

First, note that because the semantics is deterministic, we have

$$\delta = \delta_{0:n-1} \cdot \delta_{n-1} \text{ and can let } \delta_{n-1} = e \cdot \delta_n \text{ where } e \text{ is either a value or } \varepsilon$$

**Simplify goal (Gstepn):** By Definition 10 and (Hstepn) we have:

$$\langle m_0, r_0, \varepsilon, \mu_0 \rangle \xrightarrow{\delta_{0:n-1}}^{n-1} \langle m_{n-1}, r_{n-1}, \text{buf}_{n-1}, \mu_{n-1} \rangle$$

which together with (Hloweq), gives us that (IHstepn), (IHbuf), (IHreg) (IHmem) and (IHmicro) hold at step  $n - 1$ . Additionally, by Definition 10 and (Hstepn) we have:

$$\langle m_{n-1}, r_{n-1}, \text{buf}_{n-1}, \mu_{n-1} \rangle \xrightarrow{e} \langle m_n, r_n, \text{buf}_n, \mu_n \rangle \quad (\text{IHstep})$$

such that  $\delta_{0:n} = \delta_{0:n-1} \cdot e$ . Therefore, from Lemma 19 and (IHstepn), we have that:

$$(\langle m'_0, r'_0, \varepsilon, \mu_0 \rangle, \delta_{0:n}) \xleftrightarrow{n-1} (\langle m'_{n-1}, r'_{n-1}, \text{buf}'_{n-1}, \mu'_{n-1} \rangle, e)$$

Hence proving (Gstepn) amounts to showing:

$$(\langle m'_{n-1}, r'_{n-1}, \text{buf}'_{n-1}, \mu'_{n-1} \rangle, e) \xleftrightarrow{} (\langle m'_n, r'_n, \text{buf}'_n, \mu'_n \rangle, \varepsilon) \quad (\text{Gstep})$$

Consequently, we have to show that (Gstep), (Gbuf), (Greg) (Gmem), (Gmicro), (Gcorr) and (Gtrans) hold at step  $n$ .

**Transform (IHcorr):** First, observe that because the semantics is deterministic (cf. Hyp. 1), we have that:

$$\vec{c}_{n-1} = \langle m_{n-1}, r_{n-1}, \text{buf}_{n-1}, \mu_{n-1} \rangle \text{ and } \vec{c}'_\delta[n-1] = (\langle m'_{n-1}, r'_{n-1}, \text{buf}'_{n-1}, \mu'_{n-1} \rangle, \delta_{n-1}) \quad (\text{H}\vec{c}_{n-1})$$

From this, Lemma 18 and (IHcorr), we have that for all  $\text{buf} \in \text{prefix}(\text{buf}_{n-1}, \langle m_{n-1}, r_{n-1} \rangle)$  and  $\text{buf}' \in \text{prefix}(\text{buf}'_{n-1}, \langle m'_{n-1}, r'_{n-1} \rangle)$  such that  $|\text{buf}| = |\text{buf}'|$ ,

$$\langle m_{n-1}, r_{n-1} \rangle \uplus \text{buf} = \alpha_j \text{ and } (\langle m'_{n-1}, r'_{n-1} \rangle, \delta) \uplus \text{buf} = \vec{\alpha}'_\delta[j] \text{ where } j = \text{corr}_{\vec{\alpha}, \vec{c}}(n-1)(|\text{buf}|) \quad (\text{IHarch})$$

Notice that from Lemma 20, we have that the declassification trace produced by  $\vec{\alpha}$  is  $\delta$ . From Hyp. 3, it means that the observations produced by  $\vec{\alpha}$  and  $\vec{\alpha}'_\delta$  are the same. In particular, for all  $j$ , we have that

$$\alpha_j \xrightarrow{o} \_ \text{ then } \vec{\alpha}'_\delta[j] \xrightarrow{o'} \_ \text{ and } o = o' \quad (\text{Hct})$$

**Proof overview.** The proof is similar to the proof of Lemma 16. It proceeds by case analysis on the hardware evaluation, knowing that both configuration evaluate the same directive. There are two main points that differ from the proof for Lemma 16:

- First, we have to show that low-memories are equal after the evaluation of the rule RETIRE-STORE-LOW (which becomes RETIRE-STORE-PATCHED in the patched semantics);
- Second, (Gstep) requires to show that the second configuration can make a step in the *patched* execution and that the *final declassification trace is empty*. For all rules except RETIRE-STORE-PATCHED, the declassification trace that is produced is empty:

$$\langle m_{n-1}, r_{n-1}, \text{buf}_{n-1}, \mu_{n-1} \rangle \xrightarrow{\varepsilon} \langle m_n, r_n, \text{buf}_n, \mu_n \rangle$$

In the patched execution, the declassification trace is simply propagated to the next configuration. Hence the final declassification trace in the patched execution is also  $\varepsilon$ :

$$(\langle m'_{n-1}, r'_{n-1}, \text{buf}'_{n-1}, \mu'_{n-1} \rangle, \varepsilon) \xleftrightarrow{} (\langle m'_n, r'_n, \text{buf}'_n, \mu'_n \rangle, \varepsilon)$$

Notice that the rules are the same in the standard and the patched executions. Moreover, whenever we use the hypothesis Hyp. 2 in the proof for Lemma 16, we can apply the same kind of reasoning here with (IHarch) and (Hct). Hence the proof that the patch execution can actually make a step and the proofs for goals (Gbuf), (Gmem), (Greg), (Gmicro), (Gcorr), and (Gtrans) are similar to the proof for Lemma 16.

Consequently, we only need to adapt the proof of Lemma 16 for the rule RETIRE-STORE-PATCHED.

**Case RETIRE-STORE-PATCHED.** In all retire rules for store, the first instruction  $inst$  is removed from the reorder buffer:

$$buf_{n-1} = inst @ \varepsilon \cdot buf_n \text{ and } buf'_{n-1} = inst' @ \varepsilon \cdot buf'_n$$

Therefore, (Gbuf) follows from (IHbuf). Additionally, from (IHbuf) and Definition 21, we have

$$\ll inst \rrbracket_L = \ll inst' \rrbracket_L \quad (\text{Hinst})$$

From the hypotheses of the rules, we have  $inst = \mathbf{store} (a:s_a) (v:s_v)$ , meaning that  $\ll inst \rrbracket_L = \mathbf{store} \ll (a:s_a) \rrbracket_L \ll (v:s_v) \rrbracket_L$ . Therefore, from (Hinst), we have  $\ll inst' \rrbracket_L = \mathbf{store} \ll (a:s_a) \rrbracket_L \ll (v:s_v) \rrbracket_L$  meaning that  $inst' = \mathbf{store} (a':s'_a) (v':s'_v)$ . Consequently, from the hardware evaluation rules (cf. Fig. 7), the only rules that can be applied in the second configuration are the rules RETIRE-STORE-PATCHED and RETIRE-STORE-HIGH.

Additionally, we have:  $\ll (a:s_a) \rrbracket_L = \ll (a':s'_a) \rrbracket_L$  and  $\ll (v:s_v) \rrbracket_L = \ll (v':s'_v) \rrbracket_L$ , which from Lemma 9 entails  $\ll (a:s_a) \rrbracket_L = \ll (a':s'_a) \rrbracket_L$  and  $\ll (v:s_v) \rrbracket_L = \ll (v':s'_v) \rrbracket_L$ . Finally, because  $buf_n$  and  $buf_{n-1}$  are well-formed (cf. Lemma 2) and because store addresses have security level L in well-formed buffers (by Definition 16), we have  $s_a = s'_a = L$ . From  $\ll (a:s_a) \rrbracket_L = \ll (a':s'_a) \rrbracket_L$  this entails  $a = a'$ . In particular, it means that  $s_m(a) = s_m(a)$ . The proof for RETIRE-STORE-HIGH is similar to the proof for Lemma 16.

In both RETIRE-STORE-LOW and RETIRE-STORE-PATCHED, the register map is not modified. Therefore, (Greg) directly follows from (IHreg). As we have already shown (Gbuf), it remains to show (Gstep), (Gmem), (Gmicro) and (Gtrans).

(Gmicro) See Lemma 16.

(Gstep) The first execution evaluates the rule RETIRE-STORE-LOW, producing the declassification trace  $v$ . Therefore we have  $e = v$  and, from RETIRE-STORE-PATCHED,  $(\langle m'_{n-1}, r'_{n-1}, buf'_{n-1}, \mu'_{n-1} \rangle, v) \hookrightarrow (\langle m'_n, r'_n, buf'_n, \mu'_n \rangle, \varepsilon)$ , which concludes (Gstep).

(Gmem) The first execution (cf. rule RETIRE-STORE-LOW) updates its memory such that  $m_n \triangleq m_{n-1}[a \mapsto v]$  and produces the declassification trace  $v$ . Notice that from Contract 3 the declassification of  $v$  is intentional and it is secure to consider that  $m_n(a)$  is public. In the second execution (cf. rule RETIRE-STORE-PATCHED), we have  $e = v$  and the memory is updated with the declassified value  $m'_n \triangleq m'_{n-1}[a \mapsto v]$ . Therefore, (Gmem) follows from (IHmem).

(Gtrans) Notice that  $buf_n = buf_{n-1}[2..|buf_{n-1}|]$  and  $buf'_n = buf'_{n-1}[2..|buf'_{n-1}|]$ . Additionally, we have  $m_n \triangleq m_{n-1}[a \mapsto v]$  and  $m'_n \triangleq m'_{n-1}[a \mapsto v]$ , as well as  $r_{n-1} = r_n$  and  $r'_{n-1} = r'_n$ . Hence, to show (Gtrans), we need to show:

$$\mathit{transient}(\langle m_{n-1}[a \mapsto v], r_{n-1}, buf_{n-1}[2..|buf_{n-1}|] \rangle) \iff \mathit{transient}(\langle m'_{n-1}[a \mapsto v], r_{n-1}, \delta_n, buf'_{n-1}[2..|buf'_{n-1}|] \rangle)$$

This simply follows from (IHtrans), Definition 22 and Definition 17. □

**Theorem 2.** For any constant-time program up to declassification, microarchitectural state  $\mu_0$ , initial configurations  $c_0 = \langle m_0, r_0, \varepsilon, \mu_0 \rangle$  and  $c'_0 = \langle m'_0, r'_0, \varepsilon, \mu_0 \rangle$  such that  $\langle m_0, r_0 \rangle|_L = \langle m'_0, r'_0 \rangle|_L$  and number of steps  $n$ ,

$$c_0 \xrightarrow{\delta}^n c_n \implies (c'_0, \delta) \hookrightarrow^n (c'_n, \varepsilon) \wedge \mu_n = \mu'_n$$

where  $\mu_n$  and  $\mu'_n$  are the microarchitectural contexts in configurations  $c_n$  and  $c'_n$ , respectively.

*Proof.* Proof follows from the direct application of Lemma 21. □